THE STATE UNIVERSITY OF NEW JERSEY
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School of Engineering
Department of Electrical and Computer Engineering

332:223 Principles of Electrical Engineering I Laboratory
Experiment #4
Title: **Operational Amplifiers**

1 Introduction

Objectives

- To introduce operational amplifiers and dependent sources.
- To explore those circuit connections that allow operational amplifiers to operate in their linear region.

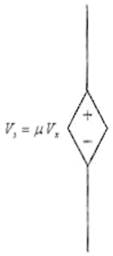
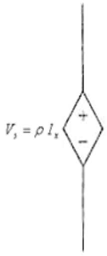
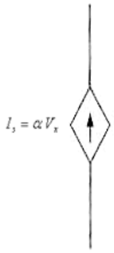
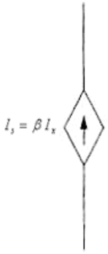
Overview

Ideal operational amplifiers (Op Amps) are two-ports (a set of two terminals is called a port) that can produce an output voltage that is directly proportional to their input voltage (linear operation). Op Amps can be operated in two ways: open loop and closed loop. The latter circuit connection is the only one that can force the Op Amp to operate in its linear region. The standard inverting and non-inverting configurations will be explored. An equivalent *circuit model* can be used to model or simulate the ideal Op Amp or to incorporate deviations from ideal behavior.

2 Theory

2.1 Dependent Sources

Dependent sources are sources whose value varies as a function of a specified voltage or current elsewhere in the circuit. The relationship could be of any form, but in this course we will introduce only those sources whose value is proportional to a voltage or current elsewhere in the circuit. Since the output quantity can be voltage or current and so can be the controlling quantity, there are four types of such dependent sources, whose names, characteristic equations, and symbols are shown in Fig. 1[1].

 Fig. 1 a Voltage Controlled Voltage Source (VCVS) $V_s = \mu V_x$	 Fig. 1 b Current Controlled Voltage Source (CCVS) $V_s = \rho I_x$	 Fig. 1 c Voltage Controlled Current Source (VCCS) $I_s = \alpha V_x$	 Fig. 1 d Current Controlled Current Source (CCCS) $I_s = \beta I_x$

2.2 Operational Amplifiers

2.2.1 Op Amp Terminal Characteristics

A 741 Op Amp is shown in Fig. 2 below. Op amps have two input terminals (input port); the input voltage V_i to the Op amps is taken across these terminals. One terminal is called inverting or negative and the voltage there is usually denoted as V_n and the other as noninverting (V_p) so that $V_i=(V_p-V_n)$. The output is taken between V_o[2] and ground. Additional terminals (such as V^+ or $+V_{cc}$, V^- or $-V_{cc}$) are used for bias, offset etc.

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[1] Note that in the characteristic equations expressed in Fig. 1, the proportionality constants μ and β are dimensionless, ρ has the units of resistance (and is called a "transresistance"), and α has the units of conductance (transconductance). Notations α, β, ρ, and μ are not necessarily standard.

[2] often signified as V_{out}

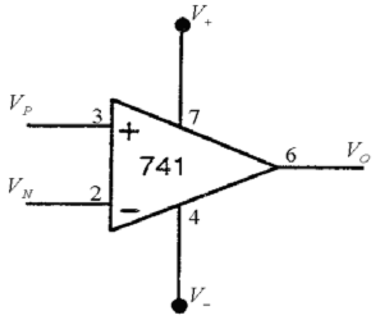

Figure 2a

The realistic model of an operational amplifier is given in your text and repeated below with equivalent notation. It involves separate input and output circuits. The input consists of an input resistance R_i between the inverting and noninverting terminal. The output consists of a voltage dependent voltage source (with voltage A_vV_i)[3] in series with an output resistance R_o. Note that the **only** connection between the input and output is through the proportionality relation of the dependent source.

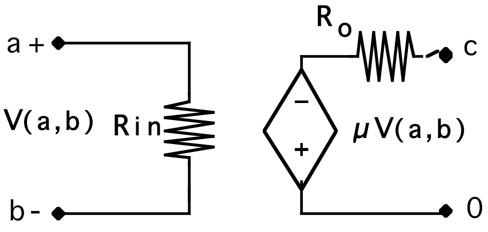

Figure 2b

The parameters involved are as follows:

1. **Input Voltage V_i**: $V(a,b)=V_i=(V_p-V_n)$.[4]
2. **Output Voltage V_o**: The output voltage of an Op Amp is proportional to the input voltage, provided it remains less in absolute value than the DC bias voltages V^+ and V^-.
3. **Input Resistance R_i** : The input resistance appears between the inverting and noninverting terminal (so that V_i appears across R_i) and can be found by dividing the input voltage V_i by the current entering the non-inverting input terminal V_p or exiting the inverting terminal V_n.
4. **Open Loop Voltage Gain μ or A_v or A**: The open loop voltage gain is the proportionality constant in the dependent source equation where $V = A_v V_i$ (or $V=\mu V(a,b)$)[5]. Different books use different notations, your text book uses A for A_v. Some other text book uses μ for A_v.

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[3] or, in the case of Fig.2b, $\mu V(a,b)$ which is the alternate notation.

[4] Op amps could be considered *differential amplifiers* because they amplify this input voltage, which is the *difference* between the voltages at the input terminals.

[5] Note that in general (i.e. if R_o is not zero) V is not equal to the output V_o whenever there exists a load R_L.

5. **Output Resistance R_o**: The output resistance appears as a resistor in series with the dependent source. In the presence of a non-zero output resistance R_o, the output voltage V_o across a load R_L is not all of $V = A_v V_i$ (or $V=\mu V(a,b)$) and can be found by analyzing the voltage divider between R_o and R_L.

2.2.2 Linear Operation and Saturation

Op Amps have two regions of operation: *linear* and *saturation*. In the *linear region*, the *voltage transfer characteristic*, i.e. the mathematical relationship between the input and output voltages, is linear. This holds true when the output voltage lies in the range $V^- \le V_o \le V^+$. From the definition of voltage gain given above, i.e. $V_o = A_v V_i$, one can see that this range corresponds to input voltages in the range of $\frac{V^-}{A_v} \le V_i \le \frac{V^+}{A_v}$. In this range the output voltage is directly proportional to the input voltage, by the factor A_v.

For input voltages outside this range, the Op Amp is said to be *saturated*, and its output is bounded by the DC bias voltages. In other words, the output voltage is clamped to V^- when $V_i<V^-/A_v$ and to V^+ when $V_i>V^+/A_v$.

2.2.3 Characteristics of an Ideal Op Amp

1. **$R_i = \infty$:** According to the definition of input resistance given above, an infinite input resistance means that no current flows into or out of the input terminals. This greatly simplifies the analysis of Op Amp circuits.
2. **$R_o = 0$:** In this case the entire dependent source voltage appears across the load resistance or as the input of another device[6].
3. **$\mu = A_V = \infty$:** If the output voltage is to be finite[7] it follows from the definition of voltage gain, that $V_i = V_o / A_v$ will go to zero if A_v is infinite. This, however, assumes that there is some way for the input to be affected by the output. Indeed this will **only** happen if there is such a connection namely a *negative feedback mechanism* in the form of *a connection between the output and the inverting terminal* (closed loop operation). If such connection does not exist, then the output will be saturated (open loop operation). For closed loop operation, it is said that a *virtual short* exists between the positive and negative input terminals[8]. This means that if an Op Amp is operating in its linear region (if it is *unsaturated*) then $V_i \approx 0$ (V_i is very close to zero), or

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[6] This is useful when cascading Op Amps to design amplifier circuits with multiple stages; this topic is covered in connection with cascading of different circuits in Principles of Electrical Engineering II .

[7] or rather unsaturated since when V_o tries to become larger than V^+ or smaller than V^- it gets clamped to V^+ or V^- respectively (or to a constant voltage somewhat less).

[8] short because there is no voltage drop but virtual because unlike real shorts there is no current flowing; remember that $R_i = \infty$ means that the input current is zero,

equivalently V_p is very close to V_n. This also simplifies the circuit calculations at the input terminals, because V_p and V_n can be represented by a single variable. When one of the two terminals is grounded, then the voltage at both the terminals is zero and the other terminal is called a *virtual ground*.

2.2.4 Building Amplifier Circuits Using Op Amps

There are two standard closed-loop connections for an Op Amp. Both have in common the connection (R_f) from the output terminal to the inverting input terminal. This connection provides *the negative feedback* and ensures the virtual short. The analysis is simple for *ideal* Op Amps since:

(a) the two input terminals are at the same voltage and
(b) there is no current into the input terminals.

The analysis usually derives a gain or amplification[9]. It is important to note that this is the gain of the *whole stage* (or the closed loop gain) and should not be confused with the gain of the Op Amp alone[10].

One last note: negative feedback does not guarantee that the amplifier will not saturate. If the input is such that the output, based on the amplification of the whole stage, is expected to be larger than the bias voltage in absolute value ($V_o > V^+$ or $V_o < V^-$) then the output *will* be clamped to V^+ (or V^-).

2.2.4.1. The Inverting Amplifier

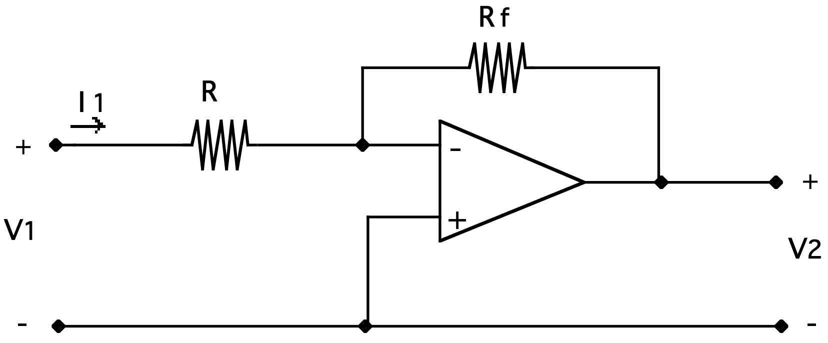

Fig. 4 Inverting Amplifier

Circuit analysis of the inverting amplifier in Fig. 4 yields the equation,

$V_2 = K\,V_1 = (-R_f/R)V_1$ (Eq. 1)

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[9] Such analyses can be found in your textbook and of course will be discussed in class.

[10] The practice of using μ rather than A_V (or simply A) for the open loop gain, and K rather than A for the gain of the whole stage aims at avoiding this confusion; this practice however is not universally used and is not adopted by your textbook. Different text books use different notations. All you need to recognize is that open loop gain of the Op-Amp is different from the gain of the entire circuit.

Thus, the theoretical gain K of the whole stage (that is, the entire Op Amp circuit of Fig 4.) is given by
$K = V_2/V_1 = (-R_f/R)$.

2.2.4.2. The Non-Inverting Amplifier

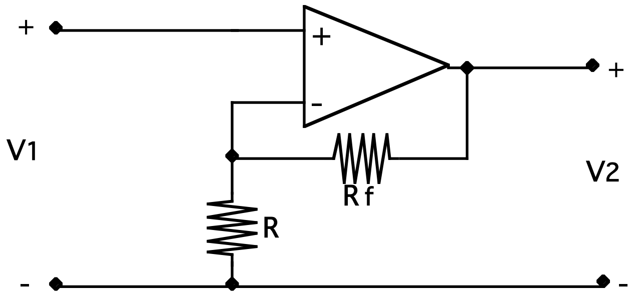


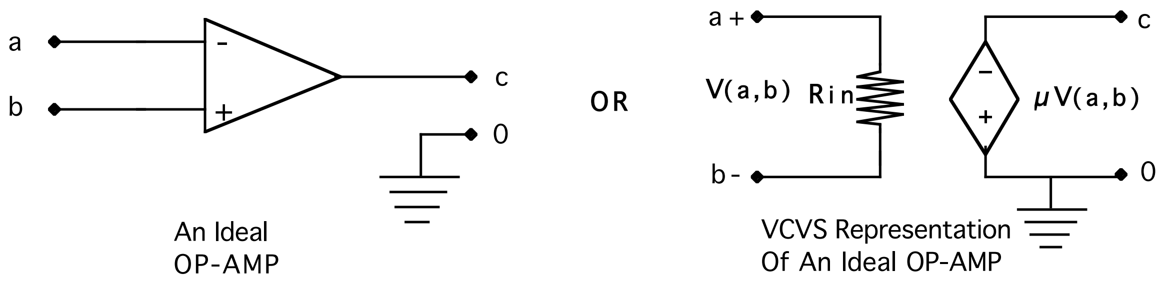
Fig. 5 Non-Inverting Amplifier

Circuit analysis of the non-inverting amplifier shown in Fig. 5 yields the equation,

$V_2 = (1+R_f/R)V_1$ (Eq. 2)

Thus, the theoretical gain K of the whole stage is given by
$K = V_2/V_1 = (1 + R_f/R)$.

2.2.5 Simulating Op Amps in PSPICE



An Ideal OP-AMP

VCVS Representation Of An Ideal OP-AMP

Figure 6

Using a VCVS, one can construct a model of the Op Amp for use in PSPICE. The circuit of Fig. 2b can be used to model a *non-ideal* Op Amp using two resistors and a dependent voltage source.
The circuit of Fig. 6 can be used for simulating an *ideal* Op Amp and is derived from Fig. 2b by shorting out the output resistor R_o (which is equivalent to setting its value equal to zero) and by picking large values for the input resistor R_i and for the Op Amp voltage gain μ (or A). Typical such values for approximating an ideal Op Amp in PSPICE are $R_i=10^{10}\Omega$ and $\mu=10^6$.

3 Prelab Exercises

Theory

3.1 Briefly explain why we assume V_p=V_n for an ideal Op Amp. What connection has to be present for this to occur?

3.2 What is the gain of an entire amplifier circuit? How is it different from the open loop gain of Op Amp?

Experiment 1

3.3 Calculate the gain **K** for the non-inverting amplifier circuit in Fig. 8 (from section 4.1 below) assuming that the Op Amp is ideal.

3.4 Calculate the theoretical linear operating range of the input voltage for the circuit in Section 4.1.

3.5 Simulate the experimental procedure of Section 4.1 in PSPICE or MULTISIM by choosing 3 different points in the linear operating range, and calculating the circuit gain at each of these points.

3.6 The PSPICE Op Amp model presented in Section 2.2.5 does not account for the effects of saturation, so you cannot simulate this portion of the experiment in PSPICE. Describe how you would expect the circuit to behave outside its range of linear operation.

Experiment 2

3.7 Calculate the gain **K** for the inverting amplifier circuit in Fig. 9 (from Section 4.2 below) assuming that the Op Amp is ideal. Your answer should be in terms of R and R_f.

3.8 Given the results of question 3.7, calculate the values of R and R_f that produce a circuit gain of -4.545 and a voltage V_i=.5V with V_s=5V.

3.9 Simulate the experimental procedure from Section 4.2 in PSPICE or MULTISIM by choosing 3 different points in the linear operating range, and calculating the circuit gain at each of these points.

4 Experiments

Suggested Equipment:
TEKTRONIX TM 503 Power Supply
2:PROTEK B-845 Digital Multimeters
741 Operational Amplifier
2:10KΩ, 2:2.2KΩ, 15kΩ, 20kΩ, 4.7kΩ
Resistance-Capacitance (RC) Box

4.1 Experiment 1: Non-Inverting Amplifier

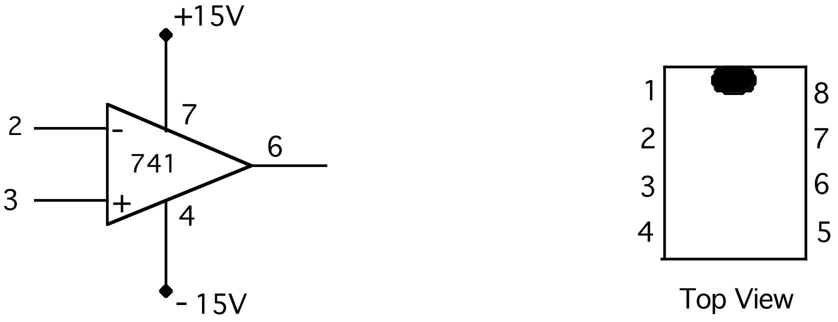


Fig. 7 Op Amp 741

You will be using the "741" Op Amp which is biased at +15V and -15V. The chip layout is shown in Fig. 7. The standard procedure on such chip packages (DIP) is to identify pin 1 as the one to the left of the notch in the chip package. The notch always separates pin 1 from the last pin on the chip. In the case of 741, the notch is between pins 1 and 8. Pins 2, 3, and 6 are the inverting input $\mathbf{V_n}$, the non-inverting input $\mathbf{V_p}$, and the amplifier output $\mathbf{V_o}$ respectively. These three pins are the only three terminals that usually appear in an Op Amp circuit schematic diagram[11].

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[11] The null offset pins (1 and 5) provide a way to eliminate any offset in the output voltage of the amplifier. The offset voltage is an artifact of the integrated circuit. The offset voltage is additive with pin $\mathbf{V_o}$ (pin 6 in this case), and can be either positive or negative and is normally less than 10 mV. Because of its small magnitude, in most cases, one can ignore the contribution of the offset voltage to $\mathbf{V_o}$ and leave the null offset pins open.

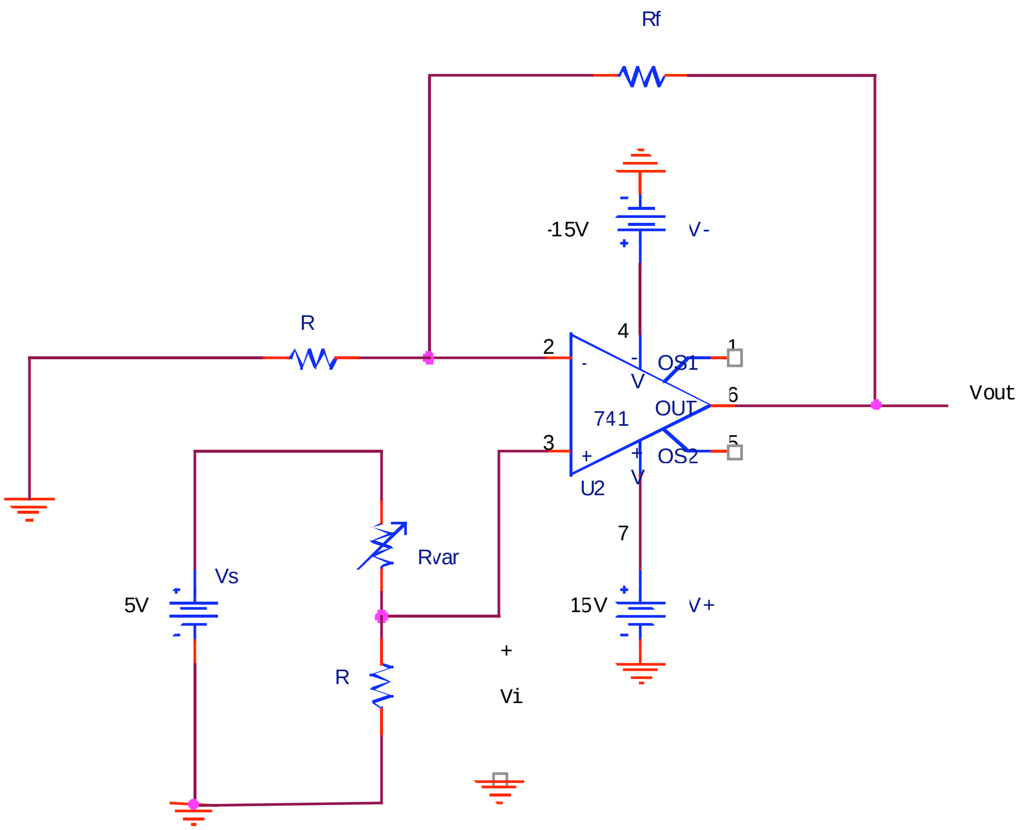

Figure 8[12]

Procedure

4.1.1 Construct the circuit in Fig. 8 with R =2.2kΩ, R_{var}=20kΩ and R_f =10kΩ.

4.1.2 Use the fixed 5V power supply of the power source for V_s. Use the RC Box in place of R_{var} and vary its value so that you can change V_i. Take readings for the output voltage V_{out} for values of V_i from -3.5V to +3.5V in increments of 0.5V and record them in Table 1. Calculate KV_i for each V_i using the calculated gain K found in prelab item 3.3 above. Calculate the % error for each row in the table.

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[12] Notice that this is identical to the non-inverting amplifier circuit shown in Fig. 5, except for the voltage divider at the non-inverting input terminal whose purpose is to decrease the input voltage and keep the Op Amp from saturating. Also shown are the connections to the DC bias supplies and the pins are labeled with their numbers.

V_i	KV_i	V_{out}	%Error

Table 1

4.1.3 For an input voltage of your choice that keeps the Op Amp in the linear region, place an ammeter in series with R_f. Record the value of the current I.

V_i =__________. I =__________.

4.1.4 Disconnect the ammeter. Keep the input voltage the same as in 4.1.3. above. Attach a load resistance between the output terminal of the Op Amp and ground. In so doing one can study the output resistance characteristics of the Op Amp. Place a 10kΩ resistor between the output terminal of the Op Amp and ground and set the supply voltage V_s to 5V. Measure the output voltage V_{out} with the DVM, and compare with the results obtained for the same input voltage in item 4.1.2. Explain any discrepancies by assuming a non-zero Op Amp output resistance. Later you will be asked to calculate the output resistance of the Op Amp based on these results.

V_i =__________. V_{out} =__________. K =__________.

4.1.5 This item involves the study of the relationship between the load resistance and output voltage (and thus also voltage gain). Keeping the source voltage at 5V, measure I_L (the current through the load resistance R_L) for each value of R_L in Table 2. Later, you will be asked to analyze this data.

R_L	I_L
10kΩ	
15kΩ	
20kΩ	

Table 2

4.2 Experiment 2: Inverting Amplifier

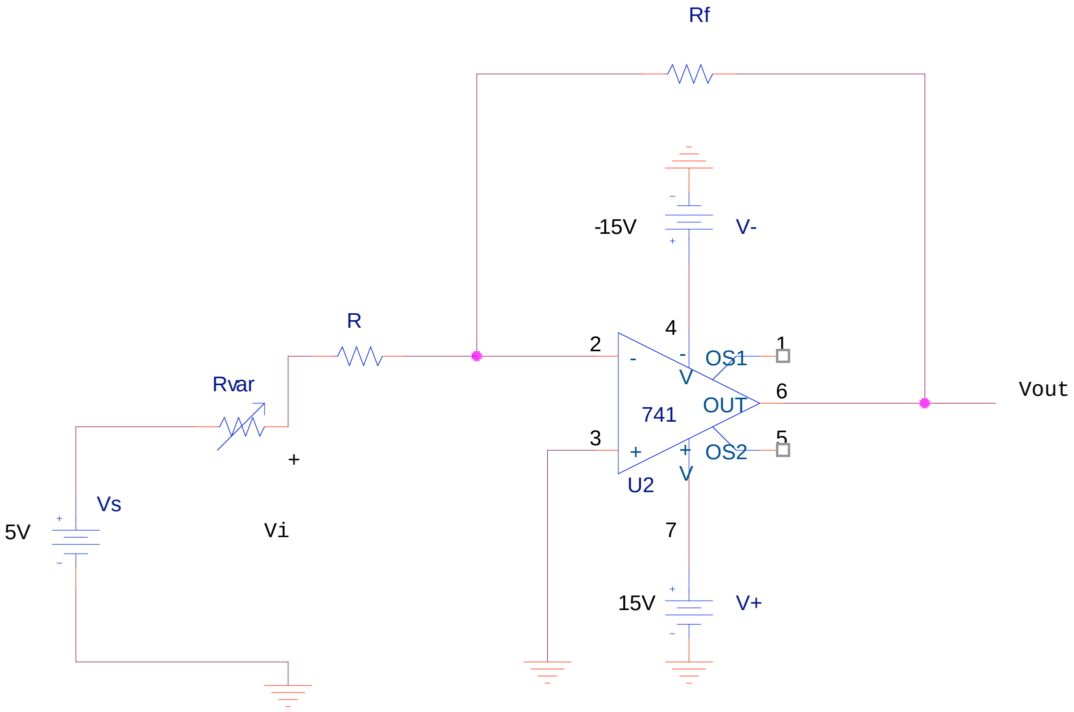

Figure 9[13]

Procedure

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[13] Notice that this is identical to the inverting amplifier circuit shown in Fig. 4, except for the mechanism to change the input voltage at the inverting input terminal. Also shown are the connections to the DC bias supplies and the pins are labeled with their numbers.

4.2.1 In prelab item 3.7 you should have calculated the values of R_f and R that yield a circuit gain of -4.545 and V_i=.5V when V_s=5V and R_{var}=20kΩ. Get your TA to check your calculations and correct them if necessary, then build the circuit of Fig. 9 with the correct values of R_f and R..

4.2.3 Use the fixed 5V power supply of the power source for V_s. Use the RC Box in place of R_{var} and vary its value so that you can change V_i. Take 21 readings for the output voltage V_{out} at each value of V_i from -5V in increments of 0.5V and record them in Table 3. Calculate KV_i for each V_i in Table 3 using the calculated gain K found in prelab item 3.7 above. Calculate the % error for each row in the table. If the measured V_{out} differs from KV_i by more than 10% you probably have an error in the circuit. Troubleshoot the circuit until it is operating properly.

Table 3

V_i	**K V_i**	**V_{out}**	**%Error**

5 Report

5.1 Derive the relationship between the current I and the resistor R_f in the non-inverter circuit of Fig. 8.

5.2 Compare the theoretical value of the gain **K =** V_{out} **/Vi** of both the inverting and the non-inverting circuits of Sections 4.1 and 4.2 that you calculated in the prelab exercises with the experimentally obtained values of gain.

5.3 Calculate the theoretical value of the current I for the resistor R_f in Section 4.1. Compare with the experimental one.

5.4 Calculate the theoretical values of the current I_L in Section 4.1.5 for all three values of R_L. Compare with the experimental ones.

5.5 Plot the experimental values of I_L vs $1/R_L$ in a graph with rectangular coordinates. From your graph, how does your output voltage depend on the load? How does the gain K= V_{out}/V_i depend on the load? Note that if V_{out} does not change with the load R_L, and since $I_L = V_{out}(1/R_L)$, then the slope V_{out} should be constant and the graph of I_L vs $1/R_L$ should be a straight line passing through the origin.

5.6 Draw two graphs of V_i vs. V_{out}, one for the inverting amplifier circuit and one for the non-inverting amplifier circuit (4.1 and 4.2). On each graph identify the transition between saturated and active regions of operation for these amplifier circuits. Label the mode of operation for each of these regions. For the active regions for both circuits, discuss the possible sources of discrepancies between the experimentally obtained value of Vout and the calculated values of KV_i.

5.7 Simulate the non-inverter circuit of Fig. 8 in PSPICE or MULTISIM for R_f = 10kΩ, R_{var}=20 kΩ and R=2.2 kΩ. Find the output voltage Vout and the current I in R_f. Assume a or μ A of 741 Op Amp.

5.8 Simulate the non-inverter circuit of Fig. 8 in PSPICE or MULTISIM for R_f = 10kΩ with the load R_L = 10kΩ applied between the output terminal of the Op-Amp and the ground. Find the current in R_L.

5.9 Simulate the inverter circuit in Fig. 9 in PSPICE or MULTISIM for R_f = 10kΩ, R_{var}=20kΩ and R=2.2 kΩ. Find the output voltage V_{out} and the current in R_f.

5.10 Simulate the circuit shown in Fig. 10 in PSPICE or MULTISIM to find i. Solve for i using nodal analysis.

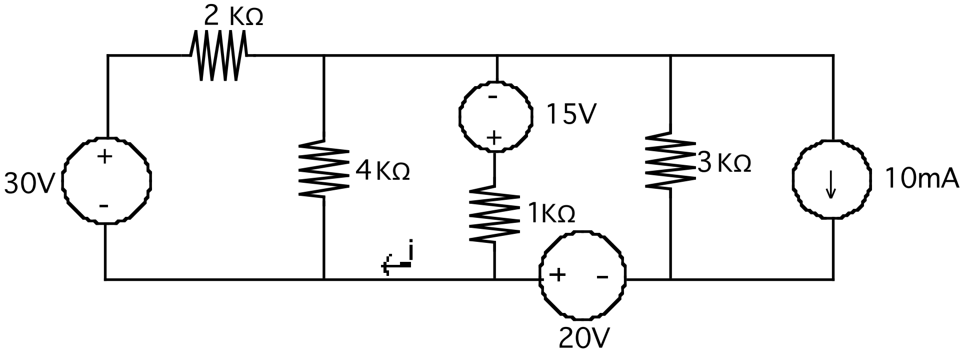

Figure 10

5.11 The circuit in Fig. 11 has been designed to implement a certain relationship between the input and output. Find the relationship and develop an alternate design using only one Op Amp.

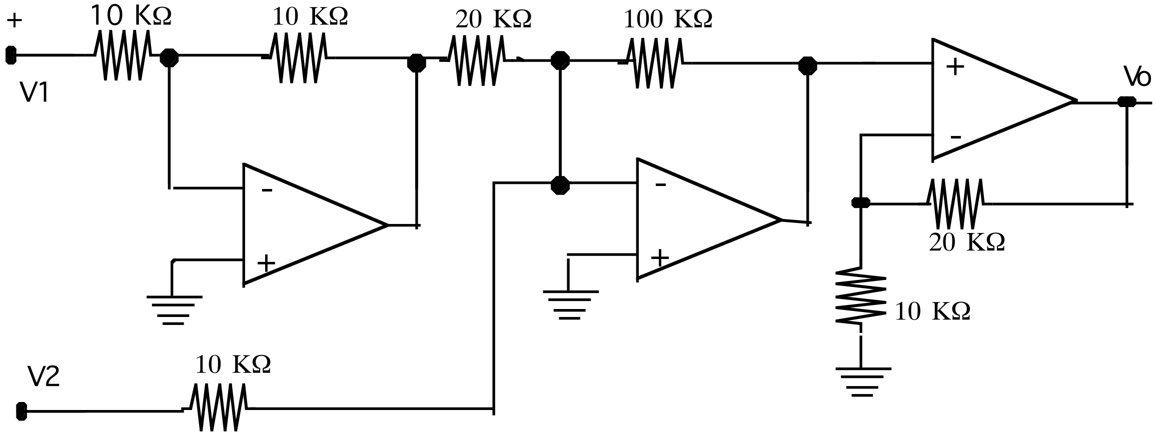

Figure 11