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DIGITAL LOGIC DESIGN

Ivan Marsic, Rutgers University
Electrical & Computer Engineering
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Lecture #9: Combinational Logic Design Practices

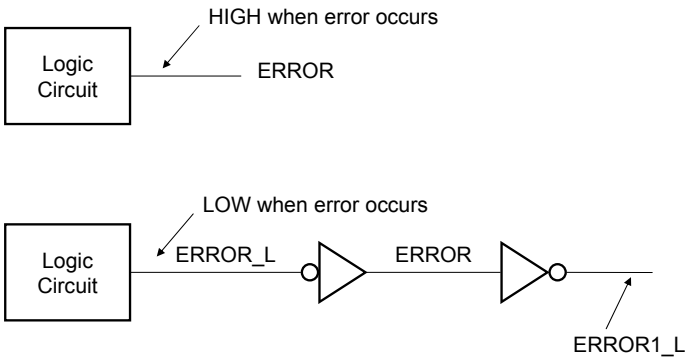
Signal Names and Active Levels

- Signal names are chosen to be descriptive
- Active levels -- HIGH or LOW
  - Named condition or action occurs in either the HIGH or the LOW state, according to the active-level designation in the name.

Active Low	*Active High*
READY–	READY+
ERROR.L	ERROR.H
ADDR15(L)	ADDR15(H)
RESET*	RESET
ENABLE~	ENABLE
~GO	GO
/RECEIVE	RECEIVE
TRANSMIT_L	TRANSMIT

we will use this notation ➔

Errors and Active Levels



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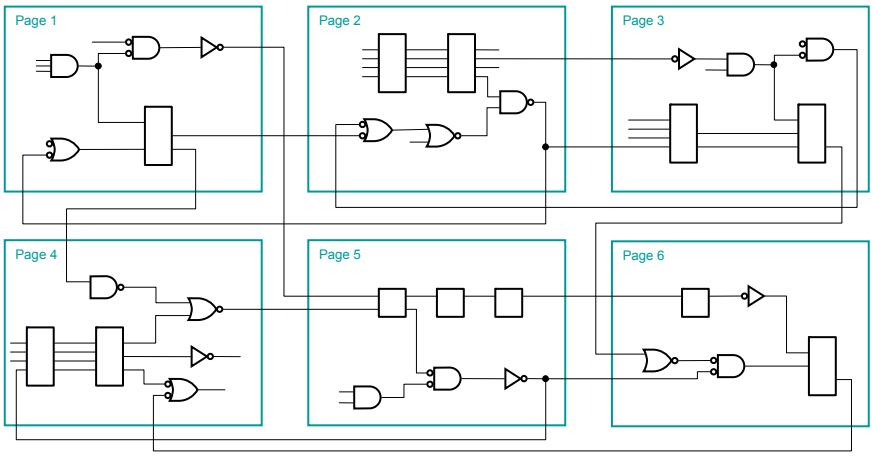
Flat Schematic Structure



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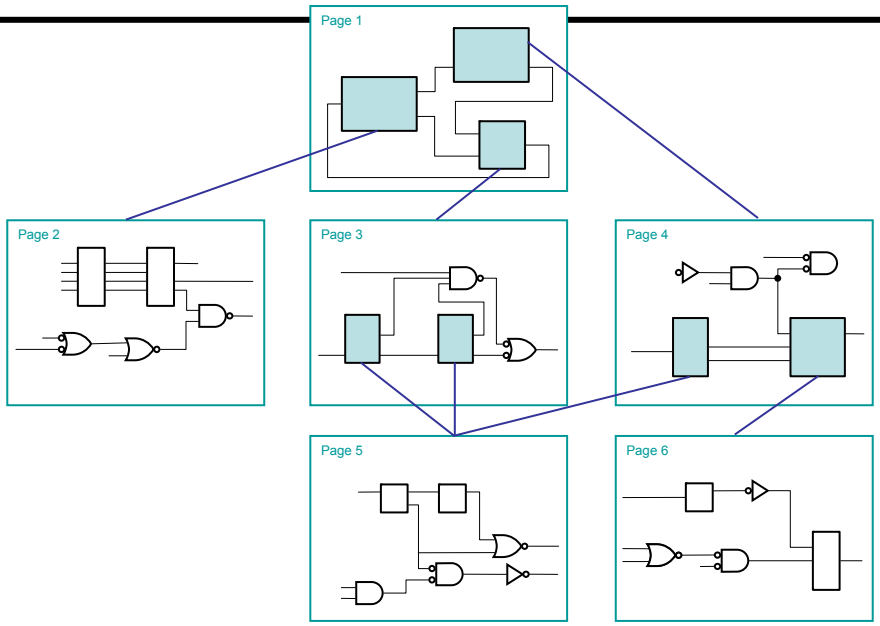
Hierarchical Schematic Structure



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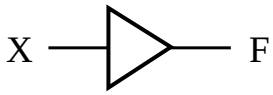
Buffer

- A buffer is a gate with the function F = X:



- In terms of Boolean function, a buffer is the same as a wire connection!
- So why use it?
  - A buffer is an electronic amplifier used to improve circuit voltage levels and increase the speed of circuit operation.

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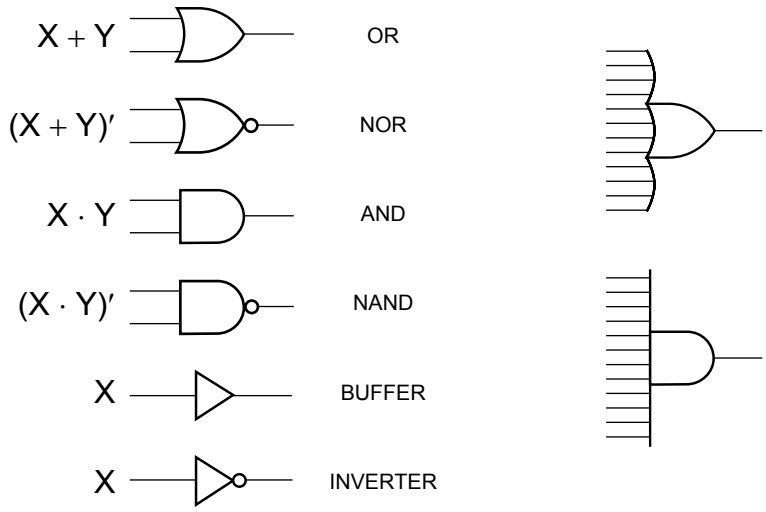
Gate Symbols [recall Lecture #4]



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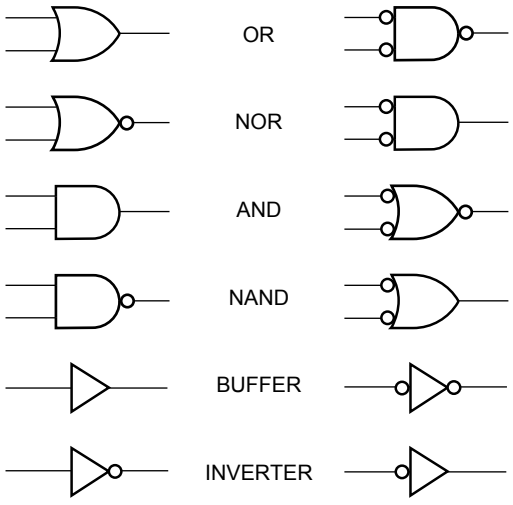
DeMorgan Equivalent Symbols [Lecture #4]



"bubble-to-bubble design"

- Which symbol to use?
- Answer depends on signal names and active levels

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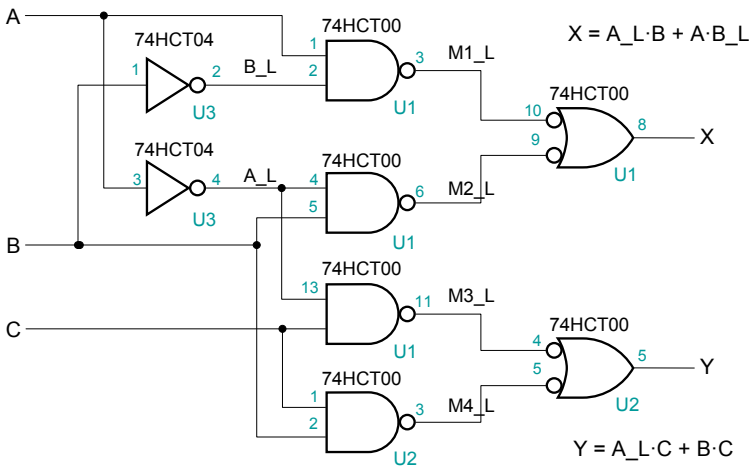
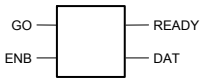
Example Schematic



HCT = high-speed CMOS
TTL compatible

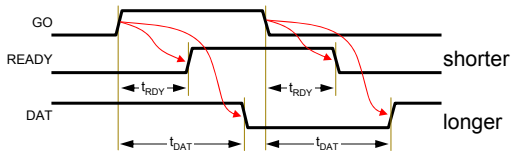
Circuit Timing

Circuit block diagram:

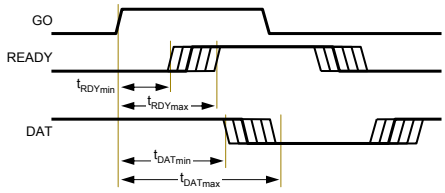


ENB (enable) is constant

causality and propagation delay:



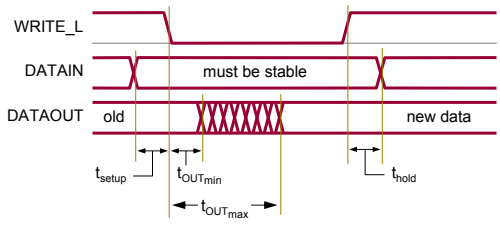
minimum and maximum delays:



another graph for the ENB input …

Timing Diagrams for "Data" Signals

Certain and uncertain transitions:



write is on "0"

Sequences of values on an 8-bit bus:

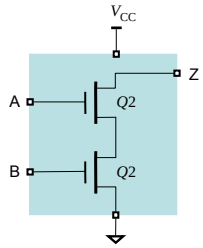
count is on "1"

Gates w/ Special I/O Characteristics

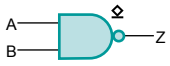
- Schmitt-trigger inputs (Wakerly, Section 3.7.2, page 130)
  - A special circuit that uses feedback internally to shift the switching threshold depending on whether the input is changing LOW-to-HIGH or HIGH-to-LOW ("hysteresis")
- Three-state outputs (Wakerly, Section 3.7.3, page 132)
  - Output has a third electrical state (not logic state), called *high-impedance*, *Hi-Z*, or *floating state*
  - In this state, the output behaves as if it isn't even connected to the circuit—the device output "floats" as if it weren't even there
- Open-drain (open collector) outputs (Wakerly, Section 3.7.4, page 133)
  - The output usually comprises an external pull-up resistor, which raises the output voltage when the transistor is turned off
  - Can be rated to withstand a higher voltage than the chip supply voltage
  - Commonly used to drive devices such as Nixie tubes, vacuum fluorescent displays, relays or motors that require higher operating voltages than the usual 5-Volt logic supply

Open-drain (open-collector) outputs

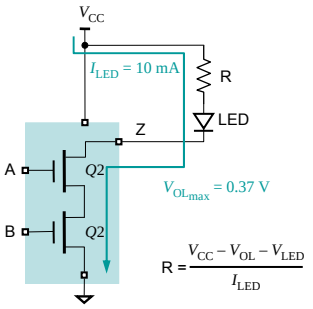
- *p*-channel transistor provides *active pull-up* of the output voltage on a LOW-to-HIGH transition
- Omitted in gates with *open-drain outputs* (see NAND gate below) [called "open-collector" in TTL]
- Example use: driving a light-emitting diode (LED)



A	B	Q1	Q2	Z
L	L	off	off	open
L	H	off	on	open
H	L	on	off	open
H	H	on	on	L



Open-drain CMOS NAND gate

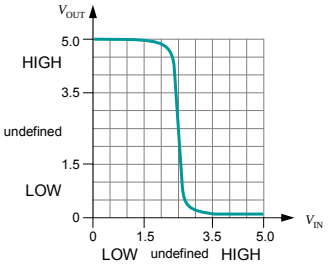


Driving an LED with an open-drain output

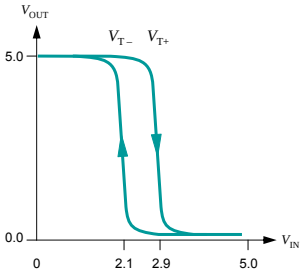
Schmitt-Trigger Inverter

It has a *hysteresis* (difference between the two thresholds) of 0.8 Volts between the low-to-high and high-to-low inputs.

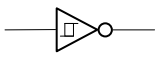
a regular inverter input-output transfer characteristic:



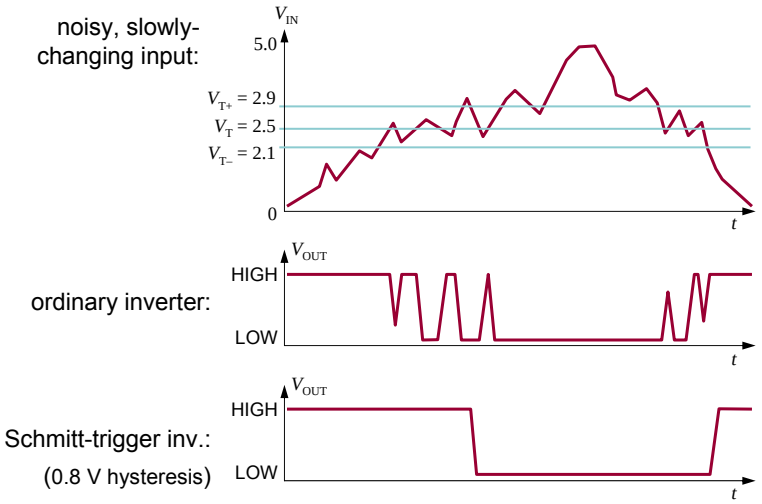
Schmitt-trigger input-output transfer characteristic:



Schmitt-trigger inverter logic symbol:

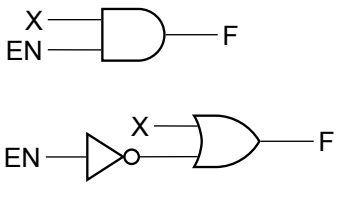


Device Operation w/ Noisy Inputs



Enabling Function

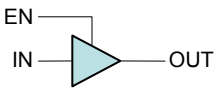
- ***Enabling*** permits an input signal to pass through a circuit to an output
- ***Disabling*** blocks an input signal from passing through to an output, replacing it with a fixed value
- The value on the output when it is disable can be Hi-Z (as for three-state buffers and transmission gates, described next), "0", or "1"
  - When disabled, "0" output
  - When disabled, "1" output



Three-State Buffers (a.k.a. Drivers)

- For the symbol and truth table, IN is the **data input**, and EN, the **control input**.
- For EN = 0, regardless of the value on IN (denoted by X), the output value is Hi-Z.
- For EN = 1, the output value follows the input value.
- Variations:
  - Data input, IN, can be inverted
  - Control input, EN, can be inverted by addition of "bubbles" to signals.

Symbol:

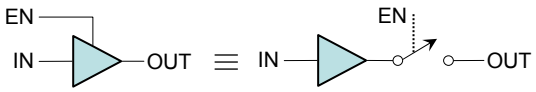


Truth table:

EN	IN	OUT
L	L	Hi-Z
L	H	Hi-Z
H	L	L
H	H	H

OUT = IN · EN

(logic function, but ignores non-logic connectivity control)



Different Flavors of Three-State

74x126

EN_L

EN_L = 1
IN = x
OUT = Hi-Z

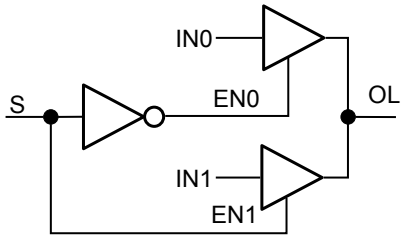
74x125

OUT_L

EN_L
OUT_L

Three-State Logic Circuit

- Normally, a logic circuit will not operate correctly if the outputs of two or more gates or other logic devices are directly connected to each other (multiple drivers conflict – "fighting")
- Use of three-state logic permits the outputs of two or more gates or other logic devices to be connected together
- Data Selection Function:
  If S = 0, OL = IN0, else OL = IN1
- Performing data selection with 3-state buffers:

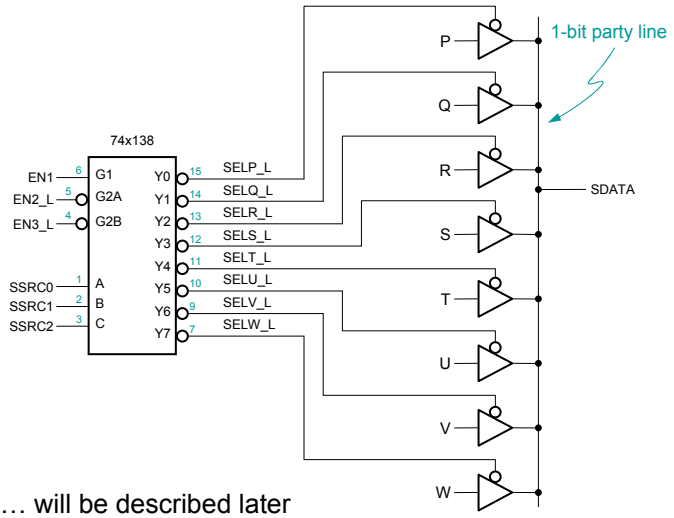


OL = IN0 · S′ + IN1 · S

- Because EN0 = S′ and EN1 = S, one of the two buffer outputs is always Hi-Z.
  (Recall: when a device output is Hi-Z, it "floats" as if it weren't even there)

8 Sources Sharing a 3-state Party Line

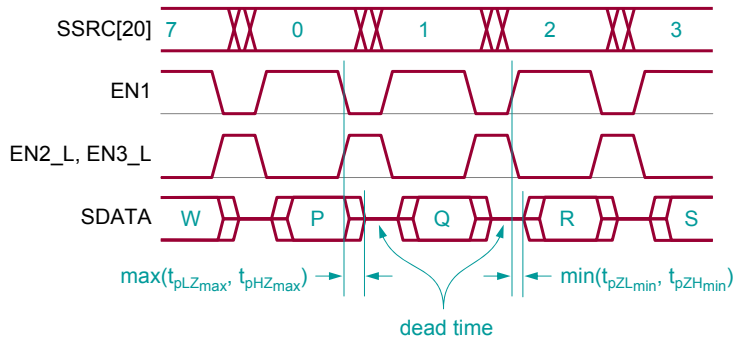
We can tie multiple outputs together, if *at most one* at a time is driven.



a decoder circuit … will be described later

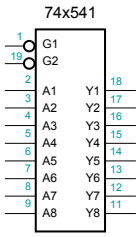
Timing Considerations

Timing considerations for the three-state party line

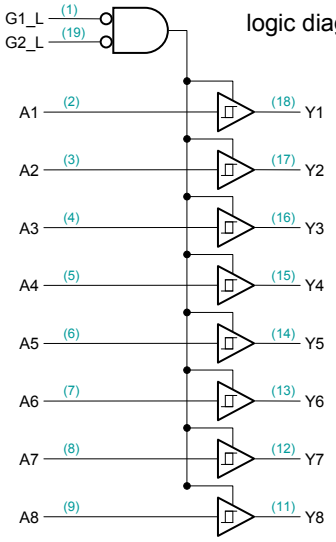


Three-State Drivers

octal three-state buffer
logic symbol



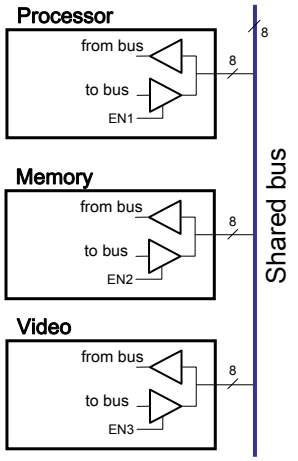
logic diagram



Note that enable inputs G1_L and G2_L simultaneously enable all eight buffers (i.e., all 8 inputs) — used in bus-based applications, described next …

Buses

- Tristate bus connecting multiple chips:



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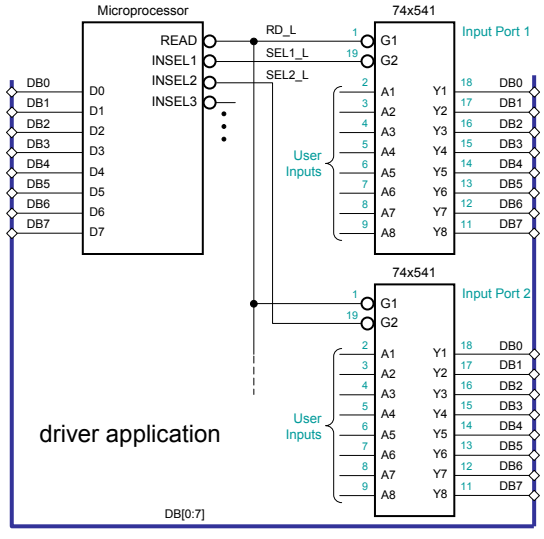
Buses - Example



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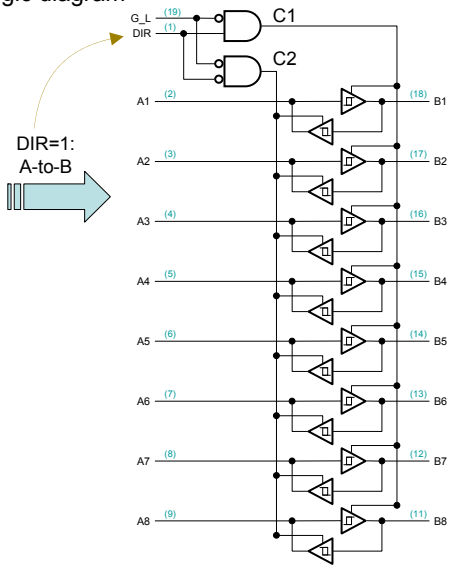
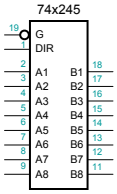
Three-State Transceivers

logic diagram



octal three-state transceiver logic symbol



enable direction

G_L	DIR	direction of transfer	C1	C2
1	x	disconnected	0	0
0	0	B → A	0	1
0	1	A → B	1	0

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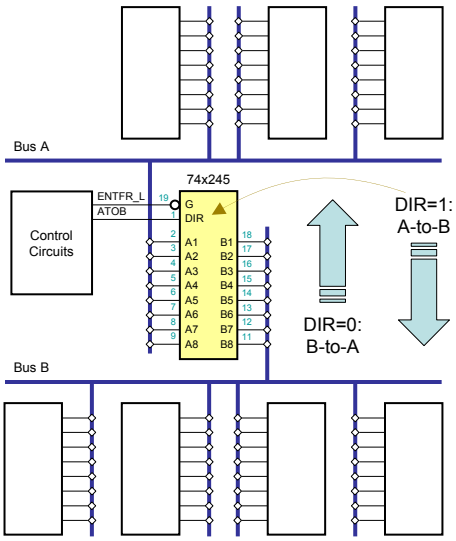
Transceiver Application

Example use of bidirectional transceiver 74x245 to control the direction of data transfer on bidirectional buses



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