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DIGITAL LOGIC DESIGN

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Electrical & Computer Engineering

Fall 2013

Lecture #5: Combinational Circuit Analysis

Combinational Circuit Analysis

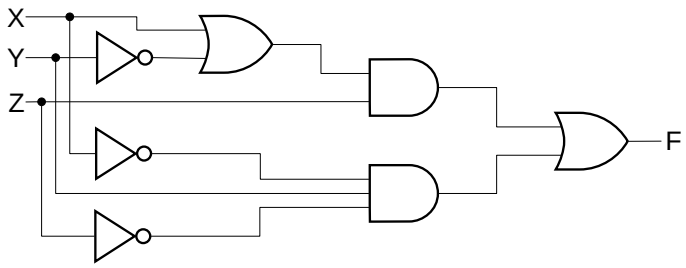
- ***Combinational circuit***: Output depends only on the current input values (called an input combination)
  - *Sequential circuit*'s output depends not only on its current input but also on the past sequence of inputs that have been applied to it.
    - I.e., a sequential circuit has *memory* of past events
- ***Combinational circuit analysis***: we are given a logic diagram and need to find its formal description (truth table, logic expression)

Kinds of Combinational Analysis

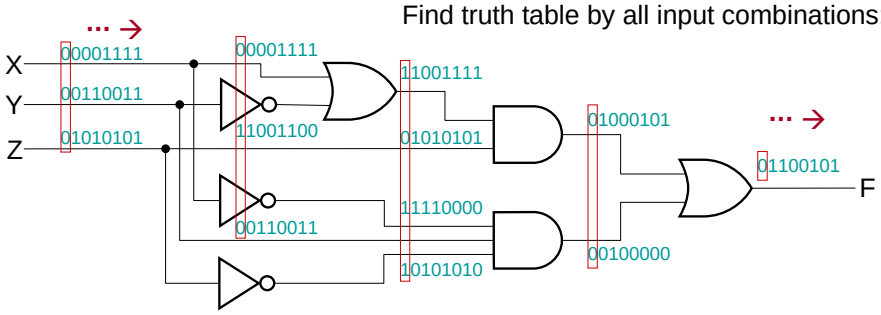
- Exhaustive (truth table)
- Algebraic (expressions)
- Simulation / test bench (in the laboratory)

Exhaustive — Truth Table

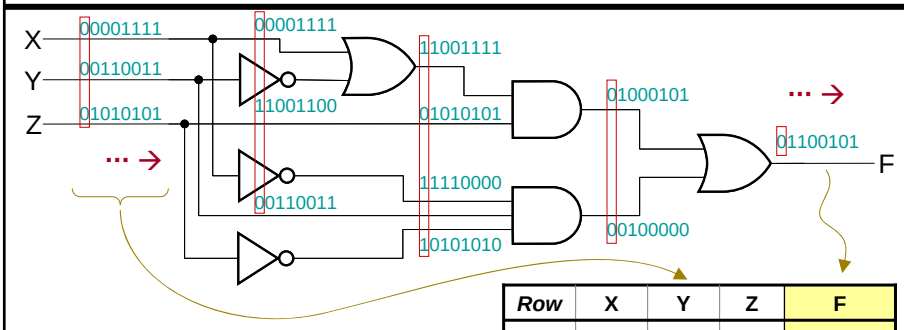
Given:



Find truth table by all input combinations:



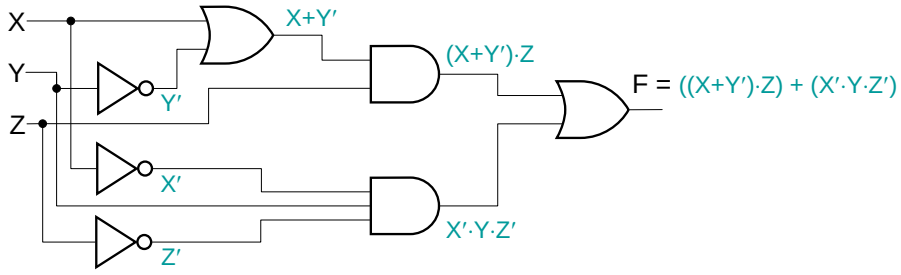
Exhaustive — Truth Table



Find truth table by all input combinations:

Row	X	Y	Z	F
0	0	0	0	0
1	0	0	1	1
2	0	1	0	1
3	0	1	1	0
4	1	0	0	0
5	1	0	1	1
6	1	1	0	0
7	1	1	1	1

Algebraic — Signal Expressions



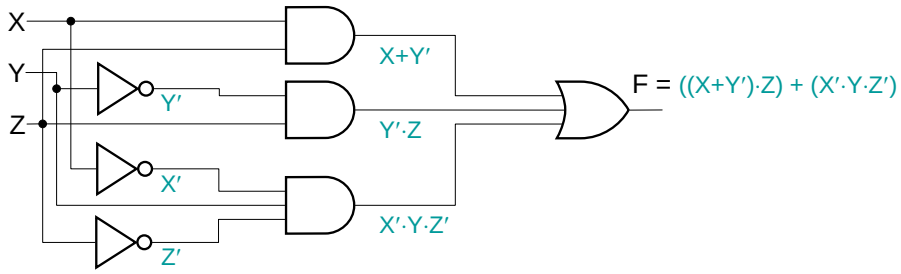
- Use theorems to transform F into another form
- E.g., “multiplying out”:

F = ((X+Y′)·Z) + (X′·Y·Z′)

= (X·Z) + (Y′·Z) + (X′·Y·Z′) …

Algebraic — Signal Expressions

…and obtain a new circuit but the same function:



Two-level AND-OR circuit

"Add out" Logic Function

"Add out" logic function is OR-AND circuit:

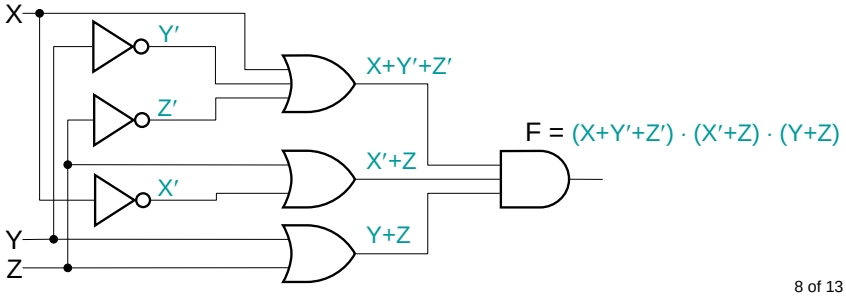
F = ((X + Y′) · Z) + (X′ · Y · Z′) ← two-level AND-OR circuit

= (X + Y′ + X′) · (X + Y′ + Y) · (X + Y′ + Z′) · (Z + X′) · (Z + Y) · (Z + Z′)

= 1 · 1 · (X + Y′ + Z′) · (X′ + Z) · (Y + Z) · 1

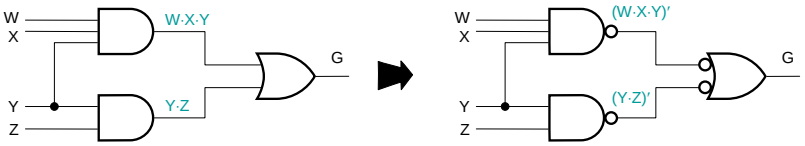
= (X + Y′ + Z′) · (X′ + Z) · (Y + Z) ← two-level OR-AND circuit

- Two-level OR-AND circuit:



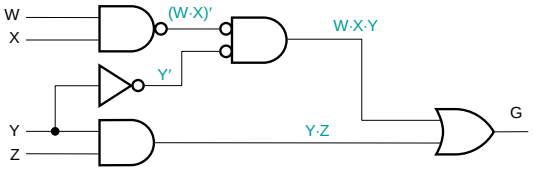
Another Example

$G(W, X, Y, Z) = W \cdot X \cdot Y + Y \cdot Z$



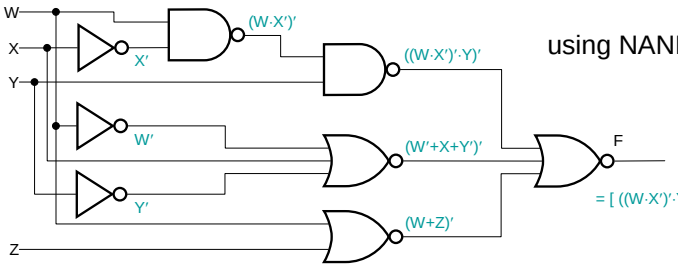
two-level AND-OR

two-level NAND-NAND



with 2-input gates only

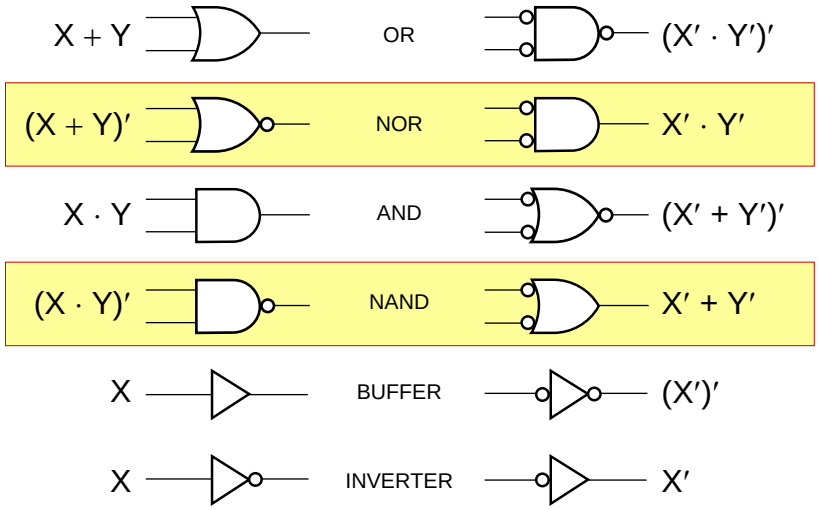
Yet Another Example (1)



using NAND and NOR gates:

$= [\ ((W \cdot X')' \cdot Y)' + (W' + X + Y')' + (W + Z)'\ ]'$

[RECALL from Lecture #4] DeMorgan Symbols



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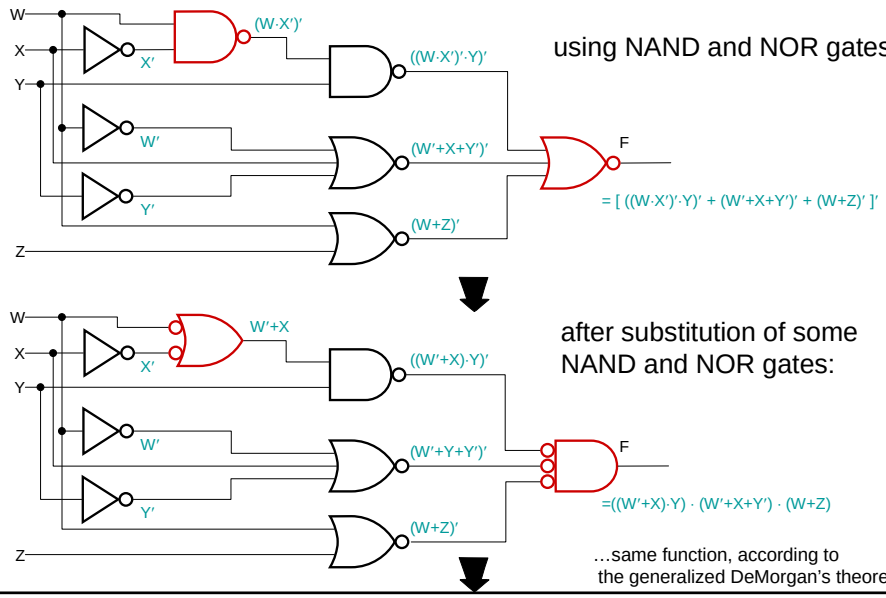
Yet Another Example (1)



Yet Another Example (2)

bubble-to-bubble:

different circuit but the same function:

here, majority are AND and OR gates