

# 14:332:231 DIGITAL LOGIC DESIGN

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Lecture #4: Boolean Algebra, Theorems,  
Standard Representation of Logic Functions

## Boolean Algebra

- a.k.a. “switching algebra”
  - Deals with Boolean values  $\rightarrow 0, 1$
- Positive-logic convention
  - Analog voltages LOW, HIGH  $\rightarrow 0, 1$
- Negative logic -- seldom used
- Signal values denoted by variables (X, Y, FRED, etc)

## Boolean Algebra is Just Like Boolean Logic ...

- NOT is a *prime* ('):
  - $0' = 1$
  - $1' = 0$
- OR is a *plus* (+):
  - $0 + 0 = 0$
  - $0 + 1 = 1$
  - $1 + 0 = 1$
  - $1 + 1 = 1$
- AND is *multiplication dot* (.):
  - $0 \cdot 0 = 0$
  - $0 \cdot 1 = 0$
  - $1 \cdot 0 = 0$
  - $1 \cdot 1 = 1$

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## Axioms (will lead to Theorems)

- Variable X can take only one of two values:  
(A1)  $X = 0$  if  $X \neq 1$                       (A1')  $X = 1$  if  $X \neq 0$
- Complement:  
(A2) if  $X = 0$ , then  $X' = 1$               (A2') if  $X = 1$  if  $X' = 0$
- Three axioms to define the AND and the OR operations:  
(A3)  $0 \cdot 0 = 0$                                       (A3')  $1 + 1 = 1$   
(A4)  $1 \cdot 1 = 1$                                       (A4')  $0 + 0 = 0$   
(A5)  $0 \cdot 1 = 1 \cdot 0 = 0$                       (A5')  $1 + 0 = 0 + 1 = 1$

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# Boolean Operators

- Complement:  $X'$  (opposite of X)
- AND:  $X \cdot Y$
- OR:  $X + Y$

X	Y	X AND Y
0	0	0
0	1	0
1	0	0
1	1	1

X	Y	X OR Y
0	0	0
0	1	1
1	0	1
1	1	1

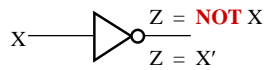
X	NOT X
0	1
1	0

- Axiomatic definition: A1 – A5, A1' – A5'

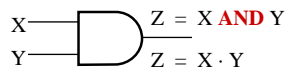
binary operators, described functionally by truth table

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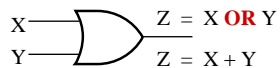
# Logic Symbols



NOT  
(complement)



AND



OR

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## Duality

- Swap 0 & 1, AND & OR
  - Result: Theorems still true
- Why?
  - Each axiom (A1 – A5) has a dual (A1' – A5')

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## Some Definitions

- *Literal*: a variable or its complement
  - X, X', FRED', CS\_L
- *Expression*: literals combined by AND, OR, parentheses, complementation
  - $X + Y$
  - $P \cdot Q \cdot R$
  - $A + B \cdot C$
  - $((\text{FRED} \cdot Z') + \text{CS\_L} \cdot A \cdot B' \cdot C + Q5) \cdot \text{RESET}'$
- *Equation*: Variable = Expression
  - $P = ((\text{FRED} \cdot Z') + \text{CS\_L} \cdot A \cdot B' \cdot C + Q5) \cdot \text{RESET}'$

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## Theorems - One Variable

(T1)	$X + 0 = X$	(T1')	$X \cdot 1 = X$	(Identities)
(T2)	$X + 1 = 1$	(T2')	$X \cdot 0 = 0$	(Null elements)
(T3)	$X + X = X$	(T3')	$X \cdot X = X$	(Idempotency)
(T4)	$(X')' = X$			(Involution)
(T5)	$X + X' = 1$	(T5')	$X \cdot X' = 0$	(Complements)

- Proofs by *perfect induction*
- Axiom (A1) is the key (a variable can take only one of two values: 0 or 1)

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## Proofs of One-Variable Theorems

(*perfect induction*)

(T3) idempotency:

$X + X = X$	$[X=0]$	$0+0 = 0$	true, according to (A4')
	$[X=1]$	$1+1 = 1$	true, according to (A3')

(T4) involution:

$(X')' = X$	$[X=0]$	$(0')' = 1' = 0$	true, according to (A2) & (A2')
	$[X=1]$	$(1')' = 0' = 1$	

Etc.

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## Boolean Operator Precedence

- The order of evaluation is:
  - Parentheses
  - NOT
  - AND
  - OR
- Consequence: Parentheses appear around OR expressions
- Example:
$$F = A \cdot (B + C) \cdot (C + D)$$

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## Theorems - Two or Three Variables

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(T6)	$X + Y = Y + X$	(T6')	$X \cdot Y = Y \cdot X$	(Commutativity)
(T7)	$(X + Y) + Z = X + (Y + Z)$	(T7')	$(X \cdot Y) \cdot Z = X \cdot (Y \cdot Z)$	(Associativity)
(T8)	$X \cdot Y + X \cdot Z = X \cdot (Y + Z)$	(T8')	$(X + Y) \cdot (X + Z) = X + Y \cdot Z$	(Distributivity)
(T9)	$X + X \cdot Y = X$	(T9')	$X \cdot (X + Y) = X$	(Covering)
(T10)	$X \cdot Y + X \cdot Y' = X$	(T10')	$(X + Y) \cdot (X + Y') = X$	(Combining)
(T11)	$X \cdot Y + X' \cdot Z + Y \cdot Z = X \cdot Y + X' \cdot Z$			(Consensus)
(T11')	$(X + Y) \cdot (X' + Z) \cdot (Y + Z) = (X + Y) \cdot (X' + Z)$			

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## Boolean Algebraic Proof - Example

$$X + X \cdot Y = X \quad \leftarrow \text{Covering Theorem (T9)}$$

Proof Steps:	Justification:
$X + X \cdot Y$	
$= X \cdot 1 + X \cdot Y$	Identity element: $X \cdot 1 = X$ (T1')
$= X \cdot (1 + Y)$	Distributivity (T8)
$= X \cdot 1$	Null elements (T2): $1 + Y = 1$
$= X$	Identity element (T1')

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## Why Theorems and Proofs?

- These theorems are useful **rules of substitution** for logic expressions
- Why substitution? —Because we may want to:
  - Design a simpler circuit (faster, easier to implement, cheaper, more reliable)
  - Use different gates for implementation (same reasons)
- Our primary reason for doing proofs is to learn:
  - Careful and efficient use of the identities and theorems of Boolean algebra, and
  - How to choose the appropriate substitution (“theorem”) to apply to make forward progress, irrespective of the application

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## Distributivity (dual)

(T8')

$$\begin{aligned}(X + Y) \cdot (X + Z) &= X \cdot X + X \cdot Z + Y \cdot X + Y \cdot Z \\ &= X + X \cdot Z + X \cdot Y + Y \cdot Z = X + X \cdot Y + Y \cdot Z \\ &= X + Y \cdot Z\end{aligned}$$

$$(X + Y) \cdot (X + Z) = X + Y \cdot Z \quad (\text{Distributivity})$$

$$(3 + 5) \cdot (3 + 7) \neq 3 + 5 \cdot 7 \quad !!!$$

parentheses, operator precedence!

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## Consensus Theorem

$$X \cdot Y + X' \cdot Z + Y \cdot Z = X \cdot Y + X' \cdot Z \quad \text{Consensus (T11)}$$

Proof Steps:

Justification:

$X \cdot Y + X' \cdot Z + Y \cdot Z$	
$= X \cdot Y + X' \cdot Z + 1 \cdot Y \cdot Z$	Identity (T1')
$= X \cdot Y + X' \cdot Z + (X + X') \cdot Y \cdot Z$	Complement (T5)
$= X \cdot Y + X' \cdot Z + X \cdot Y \cdot Z + X' \cdot Y \cdot Z$	Distributive (T8)
$= X \cdot Y + X \cdot Y \cdot Z + X' \cdot Z + X' \cdot Z \cdot Y$	Commutative (T6)
$= X \cdot Y \cdot 1 + X \cdot Y \cdot Z + X' \cdot Z \cdot 1 + X' \cdot Z \cdot Y$	Identity (T1')
$= X \cdot Y \cdot (1 + Z) + X' \cdot Z \cdot (1 + Y)$	Distributive (T8)
$= X \cdot Y \cdot 1 + X' \cdot Z \cdot 1$	$1 + X = 1$ (T2)
$= X \cdot Y + X' \cdot Z$	Identity (T1')

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## Theorems for Expressions

The theorems remain valid if a variable is replaced by an expression.

$$X \rightarrow U \cdot W$$

$$\begin{aligned} U \cdot W + Y \cdot Z &= (U \cdot W + Y) \cdot (U \cdot W + Z) = \\ &= (U + Y) \cdot (W + Y) \cdot (U + Z) \cdot (W + Z) \quad \leftarrow \text{distributivity (dual)} \end{aligned}$$

$$Z \rightarrow X'$$

$$\begin{aligned} (X + Y) \cdot (X + X') &= X + Y \cdot X' = X + Y \\ &\text{distributivity (dual)} \end{aligned}$$

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## N-variable Theorems

$$(T12) \quad X + X + \dots + X = X \quad (\text{Generalized idempotency})$$

$$(T12') \quad X \cdot X \cdot \dots \cdot X = X$$

$$(T13) \quad (X_1 \cdot X_2 \cdot \dots \cdot X_n)' = X_1' + X_2' + \dots + X_n' \quad (\text{DeMorgan's theorems})$$

$$(T13') \quad (X_1 + X_2 + \dots + X_n)' = X_1' \cdot X_2' \cdot \dots \cdot X_n'$$

$$(T14) \quad [F(X_1, X_2, \dots, X_n, +, \cdot)]' = F(X_1', X_2', \dots, X_n', \cdot, +)$$

$\uparrow$  (Generalized DeMorgan's theorem)

$\downarrow$  (Shannon's expansion theorems)

$$(T15) \quad F(X_1, X_2, \dots, X_n) = X_1 \cdot F(1, X_2, \dots, X_n) + X_1' \cdot F(0, X_2, \dots, X_n)$$

$$(T15') \quad F(X_1, X_2, \dots, X_n) = [X_1 + F(0, X_2, \dots, X_n)] \cdot [X_1' + F(1, X_2, \dots, X_n)]$$

- Prove using *finite induction*
- Most important: DeMorgan's theorems

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# DeMorgan's Theorems

Proof by *finite induction*: (basis step,  $n=2$ ; induction step,  $n=i \rightarrow n=i+1$ )

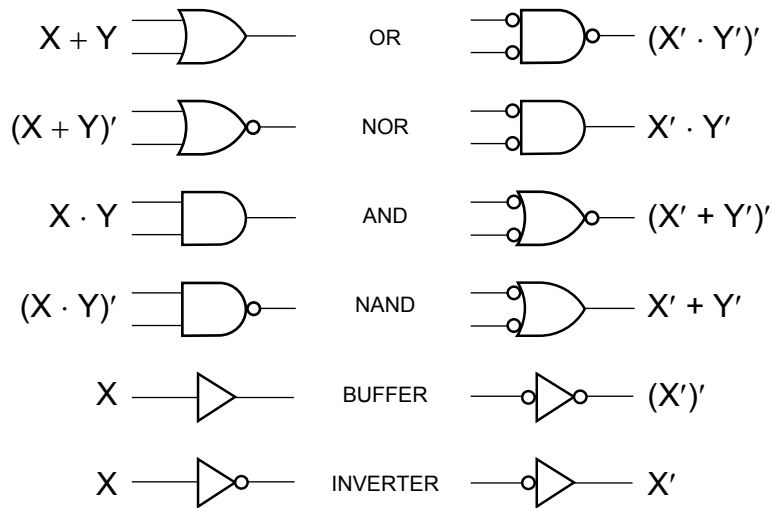
$$\begin{aligned}
 A &= X_1 + X_2 & B &= X_1' \cdot X_2' & (X_1 + X_2)' &= X_1' \cdot X_2' \\
 \text{If } A \cdot B &= 0 \text{ and } A + B = 1 & & & \text{then } A' &= B \\
 A \cdot B &= (X_1 + X_2) \cdot (X_1' \cdot X_2') & & & = 0 & \\
 A + B &= X_1 + X_2 + X_1' \cdot X_2' & & & & \\
 &= X_1 + X_2 \cdot X_1 + X_2 \cdot X_1' + X_1' \cdot X_2' & & & & \\
 &= X_1 + X_1' + X_1 \cdot X_2 & & & = 1 &
 \end{aligned}$$

} basis step

induction step { assume  $n = i$  true , then for  $n = i + 1$   
 $(A_i + X_{i+1})' = B_i \cdot X_{i+1}'$

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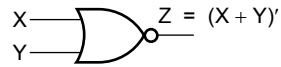
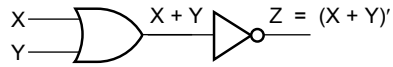
# DeMorgan Symbols



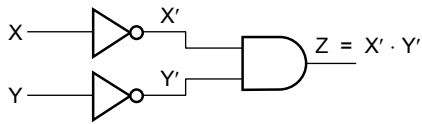
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## DeMorgan Symbol Equivalence for **NOR**

NOR



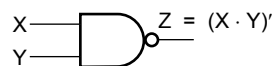
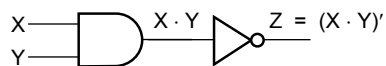
is the equivalent to



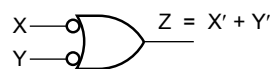
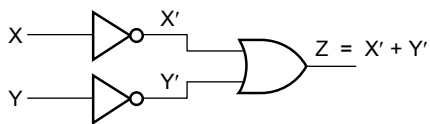
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## DeMorgan Symbol Equivalence for **NAND**

NAND

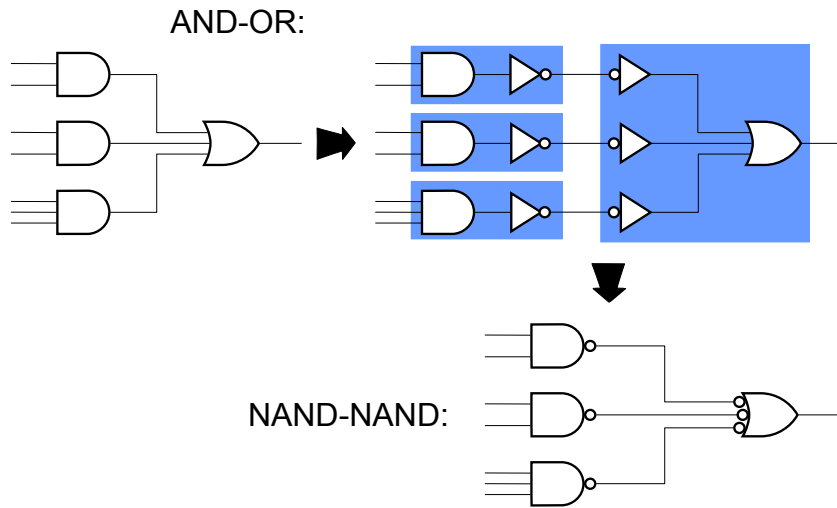


is the equivalent to



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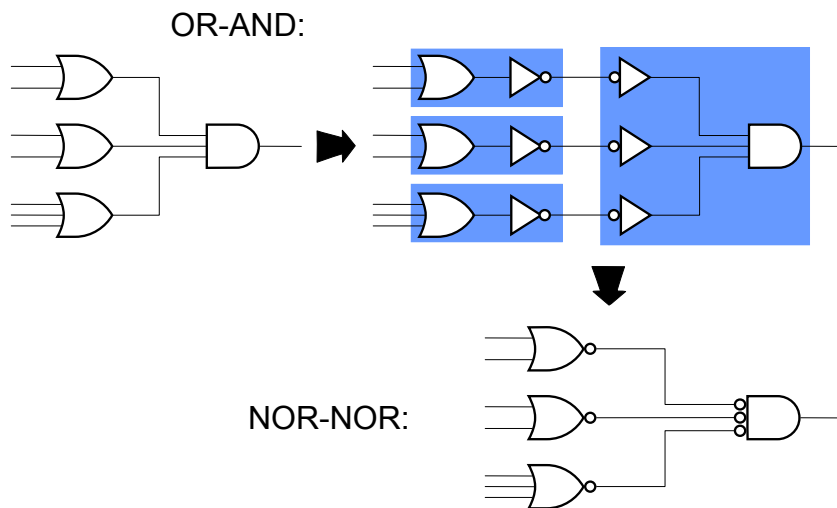
## Sum-of-Products Form



NAND-NAND preferred in TTL technology.

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## Product-of-Sums Form



Product-of-sums preferred in CMOS technology.

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