Single-Event Transient and Total Dose Response of Precision Voltage Reference Circuits Designed in a 90-nm SiGe BiCMOS Technology

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Abstract—This paper presents an investigation of the impact of single-event transients (SETs) and total ionization dose (TID) on precision voltage reference circuits designed in a fourth-generation, 90-nm SiGe BiCMOS technology. A first-order uncompensated bandgap reference (BGR) circuit is used to benchmark the SET and TID responses of these voltage reference circuits (VRCs). Based on the first-order BGR radiation response, new circuit-level radiation-hardening-by-design (RHBD) techniques are proposed. An RHBD technique using inverse-mode (IM) transistors is demonstrated in a BGR circuit. In addition, a PIN diode VRC is presented as a potential SET and TID tolerant, circuit-level RHBD alternative.

Index Terms—Bandgap reference (BGR), biCMOS circuits, PIN diode, precision voltage reference, radiation, radiation hardening by design, SiGe heterojunction bipolar transistors (HBTs), single-event transient (SET), total ionizing dose (TID), transient radiation effects, transient response.

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I. INTRODUCTION

VOLTAGE REFERENCE CIRCUITS (VRCs) [e.g., bandgap voltage references (BGRs)] are ubiquitous building blocks in a wide variety of electronic systems. The main objective of VRCs is to generate a robust and stable bias voltage that is invariant to process, supply voltage, and temperature (PVT) variations. The robustness requirements are inherently more challenging for space-based electronics, such as satellites in a geosynchronous orbit, due to exposure to the radiation-rich environment. In a space environment, the electronics experience constant bombardment by a wide spectrum of energetic photons and particles. Therefore, it is imperative to have bias circuitry that is radiation tolerant. SiGe BiCMOS technologies provide a single platform that enables a wide variety of high performance, highly integrated applications, such as monolithic microwave integrated circuits (MMICs) and system-on-chip (SoC) solutions. SiGe BiCMOS technology has been proven to be a strong candidate for these types of extreme environment applications [1], [2].

Recent investigations have reported total ionization dose (TID) and single-event transient (SET) response of SiGe BiCMOS voltage references [3]–[6]. Some of these studies concluded that SiGe BGR total dose response is dependent on the radiation source used for the exposure [3], [4], but the TID impact on the output voltage of the BGR circuit is minor. References [5] and [6] have demonstrated that SiGe HBT-based BGR circuits are sensitive to SETs. Prior studies concluded that SiGe HBTs lack of immunity is due to charge collection through the reverse-biased lightly doped p-type substrate to n-type subcollector junction [7]–[9]. Therefore, the main focus of this paper will be on the SET response of the BGR circuits and the proposed circuit-level RHBD approaches. The results presented to date were primarily focused on circuits designed in first- and third-generation SiGe BiCMOS technologies. Reference [5] proposed a SEE radiation-hardening-by-design (RHBD) technique that required device-layout modifications, but this is not a desirable approach since it increases the area and the
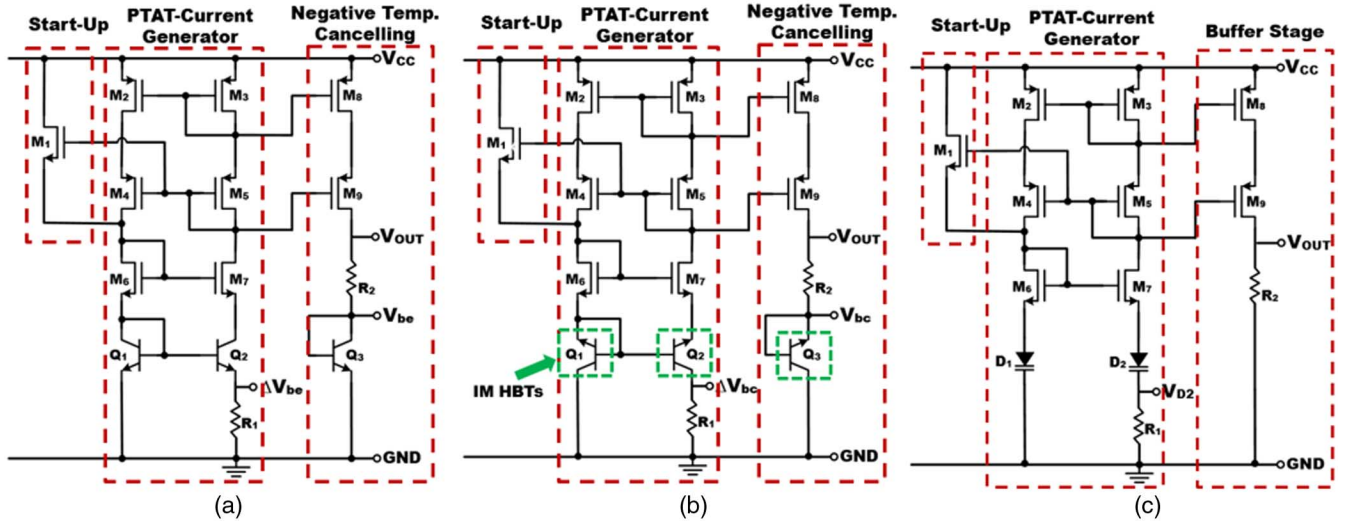
Fig. 1. Schematic diagram of the voltage reference circuits: (a) first-order BGR; (b) inverse-mode (IM) first-order BGR; and (c) PIN diode VRC.

fabrication cost. Furthermore, this proposed RHBD approach only provides partial mitigation and is likely not to be TID robust due to an additional pn junction [9].

The goal of the present work is to investigate and analyze how the VRC radiation response (both SET and TID) is impacted by technology scaling to a new fourth-generation SiGe BiCMOS technology. Based on our findings, we propose new circuit-level RHBD techniques that have little or no power, area, or cost penalty and with a high degree of immunity to SETs. The circuit-level RHBD techniques for mitigating SETs are implemented by carefully using inverse-mode (IM) transistors in the circuit while trying to maintain the overall VRC performance. We also present a PIN diode VRC as a potential SET and TID circuit-level RHBD alternative. The SET and TID responses of this new PIN-based VRC topology are compared against the first order and the IM BGR circuit topologies presented here. SET and TID response at transistor level were also measured to aid the understanding of our results. SiGe HBTs are implemented instead of Si bipolar transistors (e.g., parasitic vertical pnp) because of the enhanced performance at cryogenic temperature and the low noise capability (i.e., low 1/f noise and phase noise) [10], [11]. Both reliable cryogenic temperature operation and low noise performance are important requirements when designing electronics for space applications.

II. VOLTAGE REFERENCE CIRCUIT DESIGN

The VRCs were designed in a fourth-generation IBM SiGe BiCMOS process technology (9HP). This technology integrates 90-nm CMOS and high-speed SiGe HBTs in a single design platform. The SiGe HBT has an f_T/f_{MAX} of 300/350 GHz and an advanced back-end-of-the-line (BEOL), which includes a full suite of millimeter-wave (mm-wave) passive elements. The details of the device structure and the fabrication process are provided in [12]. The use of 300-GHz f_T devices in space electronics can enable a new integrated system solution similar to the multi-chip module remote sensor interface reported in [13] and [14].

The schematic diagrams of the three VRCs implemented in 9HP SiGe technology are shown in Fig. 1. The core of the topology for all three VRCs is based on a first-order, uncompensated BGR (i.e., no extra internal circuit is added for temperature compensation) [3]. For the purposes of this study, a simple first-order compensation topology was chosen to minimize circuit design complexity and to aid in the understanding of the circuit radiation response. The higher order BGR compensation techniques will not be discussed here but are widely available in literature. This topology consists of a startup circuit, with the M_1 transistor, followed by a bias stage where a proportional to absolute temperature (PTAT) current is generated for the next stage. This PTAT current stage is composed of transistors M_2-M_7, Q_1-Q_2, and the resistor R_1. The third and final stage cancels the negative temperature dependence of the base-emitter voltage of Q_3 with the positive voltage generated by the previous stages. This cancellation is accomplished by mirroring the PTAT current using transistors M_8 and M_9 and then passing it through resistor R_2 to generate an output voltage, V_{OUT}, which is invariant to temperature. The geometry of the SiGe HBTs Q_1 and Q_3 are $0.1 \times 2.0~\mu m^2$ and $0.1 \times 0.78~\mu m^2$, respectively. The area of the transistor Q_2 consists of three parallel copies of Q_1.

The schematic diagram of the inverse-mode (IM) VRC shown in Fig. 1(b) follows the same topology as the first-order VRC. The main difference is the use of SiGe HBTs Q_1 and Q_2 in the IM of operation (i.e., devices are operated with the collector and emitter terminals electrically swapped [15]). The results presented in [16] show that IM SiGe HBTs provide a significant improvement in circuit-level SET sensitivity. This RHBD approach has been investigated for digital circuits [15] and [17]; the present work demonstrates its application in an analog circuit. The use of IM devices required additional tuning of the device parameters (mainly resistors R_1 and R_2, and transistors M_8 and M_9) for this circuit to achieve temperature coefficient (TC) performance equivalent to that of the first-order circuit. The geometry of the SiGe HBTs Q_1 and Q_2

remained the same as the first-order BGR, but only the area of the transistor Q_3 increases to $0.1 \times 1.5 \ \mu m^2$.

The PIN diode VRC schematic diagram is shown in Fig. 1(c). The core circuit follows the same topology as the first-order VRC. However, in this circuit, the PIN diodes D_1 and D_2 replace transistors Q_1 and Q_2 in the second stage, the PTAT-current generator branch. The PIN diodes are made of a P+/N junction; the fabrication steps are similar to the extrinsic base-collector junction of the SiGe HBT. The cathode contacts are made with an N+ reach-through that wraps around the entire periphery of the anode (P+) to provide a low-impedance path to the NS subcollector and minimize series resistance in the cathode. The NS subcollector is deep trench (DT)-isolated. The D_1 and D_2 PIN diode parameters (i.e., the cathode width, the anode width, length, and the number of anode fingers) along with the R_1 and R_2 parameters were parametrically adjusted to achieve a simulated TC value that is comparable to the first-order and the IM VRCs. Both simulation and measurement results showed that the generated PTAT current using PIN diodes varies less with temperature in comparison to the SiGe HBT-based VRCs. For this circuit, a first-order temperature compensation was not implemented for the purpose of minimizing the circuit complexity and to enable a direct radiation response comparison with the other two VRCs, the first-order and the IM VRCs. The main implication of this design choice is that the output voltage displays a PTAT slope that yields a higher TC. All three circuits were designed for operation with a power supply voltage of 2 V. The supply voltage was chosen to meet the circuit voltage headroom requirement since cascode current mirrors were implemented to improve the power supply rejection (i.e., the amount of noise from a power supply that a circuit or device can reject).

III. EXPERIMENTAL DETAILS

Three different radiation experiments were performed. In the first experiment, SET measurements were conducted at the Naval Research Laboratory using the two-photon absorption (TPA) backside pulsed laser system. This setup is identical to that reported in [18]. The system is capable of producing a 1.2 μm full-width half-maximum (FWHM) spot size diameter charge distribution profile [19]. The system provides the ability to perform 3-D position-dependent (XYZ) time-resolved SETs nondestructively in a laboratory setting. The TPA system was configured to produce optical pulses at 1260 nm at a frequency of 1 kHz, with a pulsewidth of approximately 120 fs. The laser-induced transient waveforms were captured using a high-speed high-bandwidth Tektronix DPO71254 12.5-GHz, 50-GS/s real-time oscilloscope. The voltage reference circuits under test were packaged using a high-speed custom-designed printed circuit board (PCB). The translation platform used to secure the PCB has a 0.1-μm position resolution in all three axes, XYZ. All data were collected in a rectangular XY grid at a fixed Z position. For each measurement, the Z position was optimized to place the sensitive volume at the focus of the laser beam. A detailed description of the measurement system can be found in [20].

For the second and third experiments, the total dose exposures were conducted at Vanderbilt University using an ARACOR 10-keV X-ray source and a 2-MeV Pelletron (proton) source.
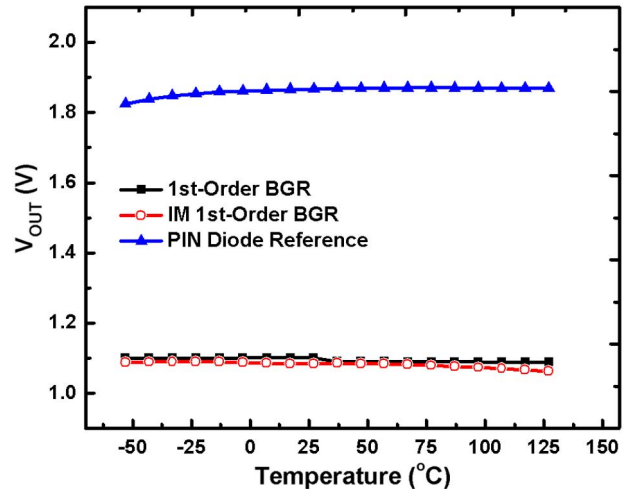

Fig. 2. Output voltage as a function of temperature for the three voltage reference circuits: first-order BGR, IM first-order BGR, and PIN diode voltage reference.

For the 10-keV X-ray experiments, the samples were mounted on 28-pin ceramic dual-in-line packages and irradiated at a dose rate of 31.5 krad (SiO_2)/min or 525 rad(SiO_2)/s. The measured equivalent total dose for the 10 keV X-ray experiment started at 100 krad(SiO_2) and was incrementally increased to a final value of 6 Mrad(SiO_2). For the low energy proton irradiation, the samples were packaged using the same high-speed custom-designed printed circuit board as used in the SET experiments. The samples were irradiated at various total dose levels, starting at 33 krad(Si) (proton fluence of 4.92×10^{10} p/cm^2), to a TID of 2 Mrad(Si)(proton fluence of 1.97×10^{12} p/cm^2). The voltages and current biasing were monitored and measured *in-situ* using Keithley dc supplies and Agilent digital multimeters. For all three experiments, the samples were irradiated at room temperature under normal operating conditions. For both TID experiments, a total of six samples were irradiated and measured (i.e., two of each VRC).

IV. RESULTS AND DISCUSSION

A. SET VRC Response

All of the circuits and devices were characterized before irradiation. The measured pre-irradiation output voltages for all three VRCs are shown in Fig. 2. All three VRCs demonstrate acceptable performance across temperature. As previously stated, temperature compensation was not implemented for the PIN diode VRC. The impact of this design choice is observed in Fig. 2 (closed triangle symbols); the output voltage decreases with decreasing temperature ($< 0 \,^{\circ}C$). The data presented here are for one of the packaged samples; these are representative of the data set measured across all the samples.

To investigate SETs in the VRCs, the TPA system was used to perform 2-D raster scans on all of the devices while monitoring the key nodes in the circuits, V_{CC} and V_{OUT}, and also two internal nodes V_{BE} and ΔV_{BE} for the first-order BGR, V_{BC} and ΔV_{BC} for the IM BGR, and V_{D2} for the PIN VRC. Sensitive devices responsible for generating transients with large peak magnitudes and duration were identified. Fig. 3
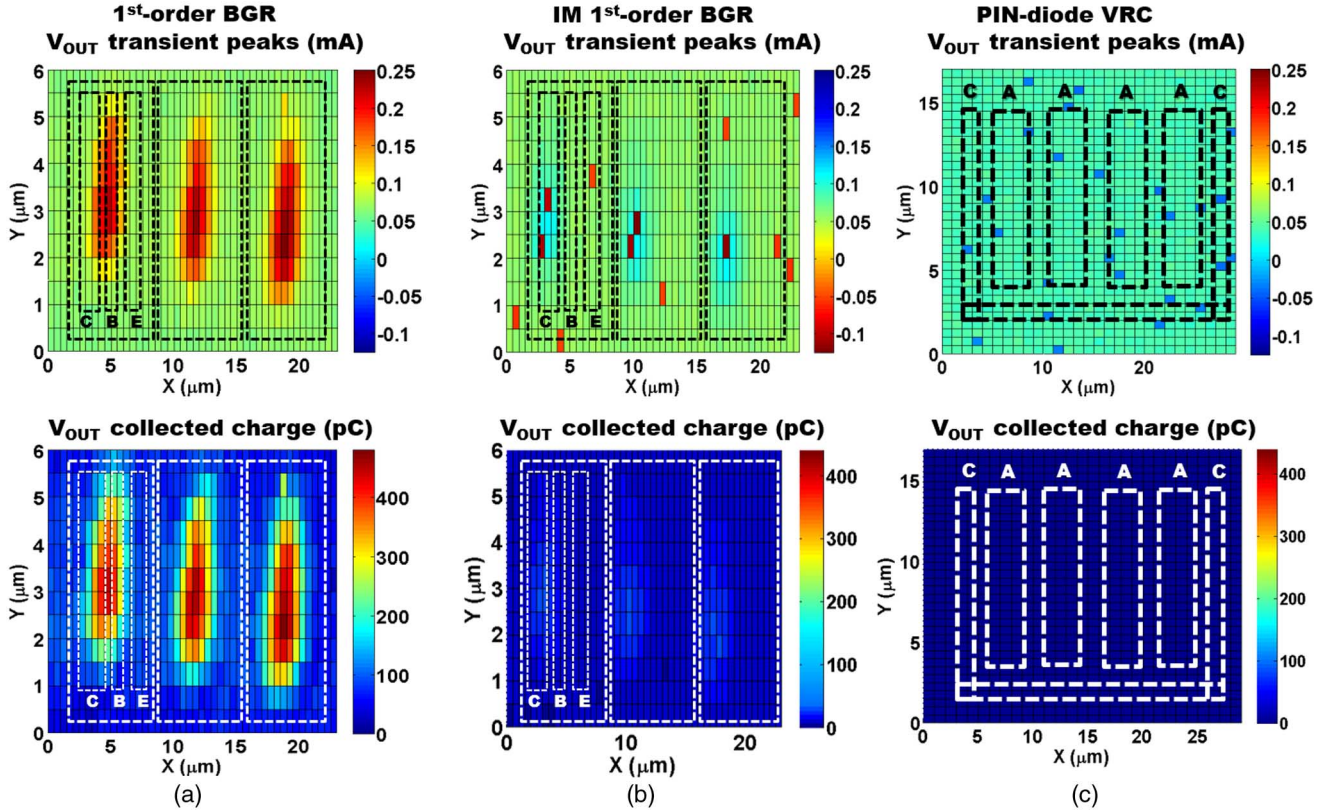
Fig. 3. Measured peak transient currents (in top row) and collected charge (in bottom row) at the V_{OUT} terminal as a function of position resulting from a laser strike on (a) a first-order BGR circuit Q_2 transistor, (b) an inverse-mode BGR circuit Q_2 transistor, and (c) a D_2 device in the PIN diode voltage reference circuit, for an incident laser energy of 31 pJ.

illustrates the recorded peak currents and the corresponding collected charge at the output terminal V_{OUT} as a function of the incident laser position. The most sensitive devices were determined after initial raster scans on all non-FET devices. For both the first-order and IM BGRs, the raster scans revealed that the most sensitive device is Q_2. Q_2 consists of three parallel copies of Q_1 with an emitter area of (A_E) $0.1 \times 2\ \mu m^2$. For some of the raster scans, the sensitive areas appear larger than the actual device geometry. This discrepancy likely arises from the large pulse irradiance used for this set of experiments coupled with the finite spot size of the laser pulse. The apparent size of the sensitive area is a consequence of the overlap of the tails of the Gaussian laser pulse profile with the sensitive region of the devices [21].

As anticipated, the first-order BGR demonstrated greater sensitivity in its SET response [Fig. 3(a)] when compared to the IM BGR and the PIN diode VRC, as shown in Fig. 3(b) and (c), respectively. From these results, a worst-case transient peak current of ≈ 0.2 mA and a corresponding collected charge of ≈ 400 pC at the V_{OUT} terminal [Fig. 3(a)] were measured. The captured transients at the V_{CC} terminal (not shown here) follow an identical response as the ones recorded for the V_{OUT} terminal, with the only difference being the opposite polarity of the transients and collected charge. Fig. 3(b) depicts the measured 2-D raster scan response of the IM BGR. The results indicate a significant reduction of the total sensitive area as seen by the decrease in the transient peaks and the corresponding collected charge when compared to the first-order BGR response.

The time-resolved transients at similar $X - Y$ positions are shown in Figs. 4(a) and 5(a) for both the first-order and the IM BGRs, respectively. These figures provide additional information that cannot be ascertained simply from 2-D raster scan responses. The results show that the measured peak transient current at the V_{OUT} and V_{CC} terminals of the IM BGR [Fig. 5(a)] is reduced by approximately 0.1 mA in magnitude, when compared with the first-order BGR. The transient duration for the first-order and IM BGRs are also plotted in Fig. 4(b) and Fig 5(b), respectively. From these two plots, the full-width at half-maximum (FWHM) duration were extracted from the measured transient signals at the V_{OUT} terminal for both first-order and IM BGRs, and the values were ≈ 600 ns and ≈ 0.7 ns, respectively. The FWHM duration decreases by approximately three orders of magnitude. These results confirm that the proposed IM circuit-level RHBD technique can be used for SET mitigation on this type of ubiquitous analog circuit.

The observed decrease in transient peak current, transient duration, and collected charge occurs because the electrical collector (physical emitter) of the IM SiGe HBTs are electrically isolated from the sensitive subcollector-substrate junction [15]. This isolation leads to a reduction in the ion-shunt region (two linked junctions due to high-injection concentrations of excess carriers) since the electrical collector current is no longer a superposition of the emitter-collector ion-shunt and substrate diffusion current, thus reducing the overall transient peaks magnitude and the reduction in transient duration at sensitive circuit nodes [16]. The reduction in total transient duration is at-
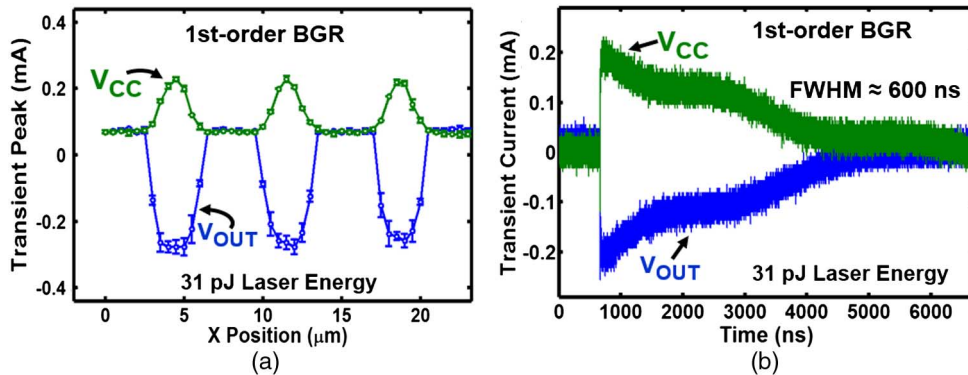
Fig. 4. First-order BGR: (a) transient peaks over the width of the device and (b) transient current of the resulting transient captured at the V_{OUT} and V_{CC} terminals from laser strikes on Q_2 (SiGe HBT), with an incident laser pulse energy of 31 pJ.

tributed to both the absence of the subcollector-substrate diffusion tail and the ion-shunt region as shown in [16]. Reference [16] provides an in-depth study of the contributions related to the oxide trapped charge and the interface traps in the shallow trench isolation (STI) for both forward- and inverse-mode SiGe HBTs fabricated in the 90-nm SiGe BiCMOS process.

The 2-D raster scan response from laser strikes on diode D_2 of the PIN VRC is shown in Fig. 3(c), and no transients are observed at either the V_{OUT} or V_{CC} terminals. The measured collected charge at V_{OUT} are < 0.2 pC, a calculated value that is within the noise floor capability of the measurement equipment (Tektronix oscilloscope). Current transients of ≈ 0.2 mA in magnitude were captured at the cathode terminal V_{D2} (not shown here) as 2-D raster scans were performed. However, it was determined that the observed transient signals do not propagate to the V_{OUT} and V_{CC} terminals because the PIN diode is forward biased. Under this bias condition, only a small amount of charge is collected at the anode terminal from the laser strikes due to the small electric field present that limits the charge separation. Thus, any electron–hole pairs generated from the laser strike quickly recombine in the space charge region and charge collection is minimized at the anode. In addition, charge collection at the anode is further minimized because the P+ region is DT-isolated.

Also, Cadence simulations confirm that the PIN diode is forward-biased with ≈ 0.8 V and ≈ 70 μA across the device. Under this bias condition, the PIN diode presents a large resistance at the source of nFET transistor M_7 [Fig. 1(c)]. The parasitic capacitances from the nFET transistor and the PIN diode, along with this large resistance, act as a filter for the transients resulting from laser strikes on D_2. A total of four samples were exposed for two separate experiments, and the results reveal that this VRC is insensitive to SETs, clearly an important result. The proposed RHBD approach using PIN diodes instead of IM SiGe HBTs provides complete immunity to SETs at the circuit level.

B. TID VRC Response

The results from 10-keV X-ray and 2-MeV proton irradiation of the first-order BGR are shown in Fig. 6(a) and (b), respectively. As previously reported in [4], the TID response of the first-order BGR is radiation source dependent. The measured data indicate that total dose effects are minor for these circuits and that higher output voltage changes are observed for the samples exposed to X-rays. The first-order BGR V_{OUT} shows a worst-case change of about 2.5% (≈ 28 mV). The primary reason for the change in V_{OUT} is the excess base leakage current generated in the SiGe HBTs. This excess base leakage current is demonstrated by the observed trends of the measured V_{BE} and ΔV_{BE} voltages shown as open circle and open triangle symbols in Fig. 6(a), respectively. This increase in base current is due to radiation-induced G/R traps located at the EB oxide spacer [22]. The base current increase was also verified by performing pre- and post-irradiation dc characterization of individual transistors with similar A_E and at similar operating bias points as the devices in the VRCs (data not shown here for brevity).

For the 2-MeV proton irradiation, the observed changes are less than 0.1%. These dc results are consistent with the measured forward Gummel characteristics (data not shown here for brevity). The radiation source dependency can be attributed to fundamental differences in the local recombination rates in the emitter-base and STI interface regions [23]. Standalone test structures confirm that for a V_{BE} bias voltage of ≈ 0.8 V, the change in base current is minimal with increased proton irradiation dose. IM BGRs were irradiated under similar conditions as the first-order BGR, and the results are shown in Fig. 7 (open circle symbols). Similar to first-order, the IM BGR exhibits worst case V_{OUT} change for the samples exposed to X-rays as shown in Fig. 7(a) (open circle symbols). The V_{OUT} terminal shows an average change of $\approx 1.5\%$ as total dose increased to 6 Mrad(SiO$_2$). This approximate change is attributed to a small increase in the base current of the SiGe HBT with increased TID. The inverse Gummel results of irradiated standalone IM SiGe HBTs confirms that the base current for a V_{BC} bias voltage of ≈ 0.8 V displays very small changes (from ≈ 250 pA to ≈ 380 pA) with increased dose, thus the nearly constant BGR output percentage change. The 2-MeV proton measured response for the IM BGR shown in Fig. 7(b) (open circle symbols) reveals that the change in V_{OUT} is less than 1% at a total dose of 1.9 Mrad(SiO$_2$). The change in V_{OUT} displays an increasing trend with increased total dose. This may result from the fact that both ΔV_{BC} and V_{BC} increase with dose, according to the measured data not shown here. The base-collector voltage ΔV_{BC} of transistor Q_2 is related to the
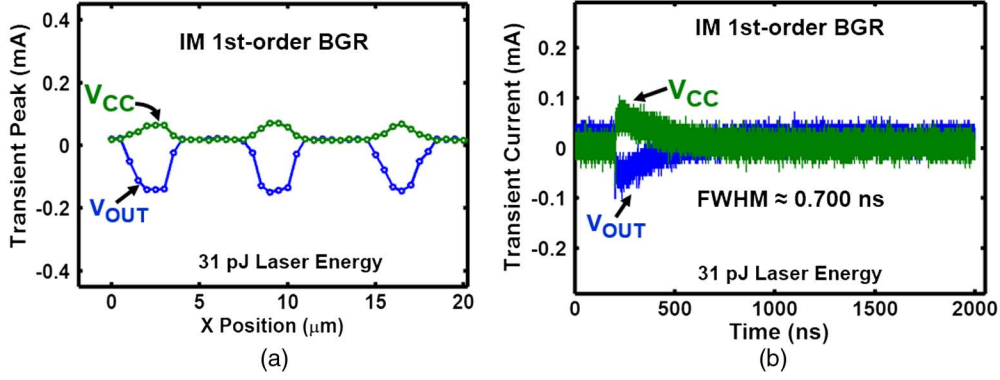
Fig. 5. Inverse-mode (IM) first-order BGR: (a) transient peaks over the width of the device and (b) transient current of the resulting transient captured at the V_{OUT} and V_{CC} terminals from laser strikes on Q_2 (SiGe HBT), with an incident laser pulse energy of 31 pJ.
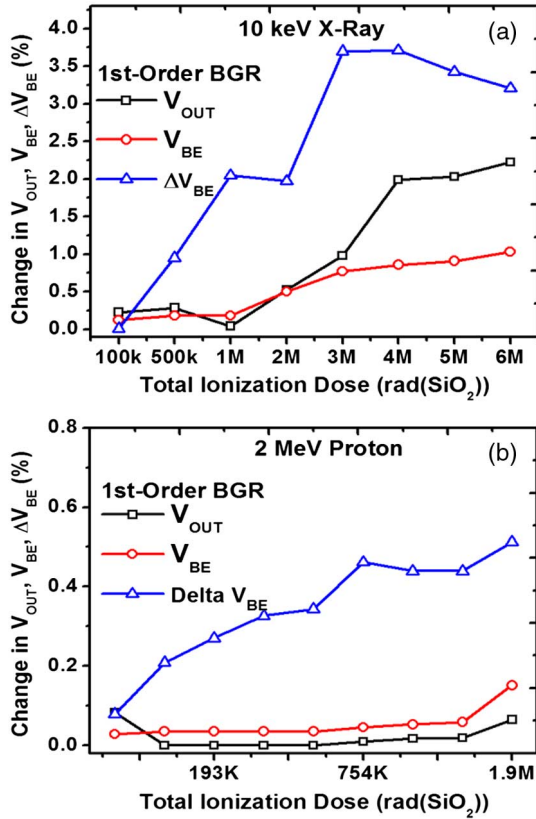

Fig. 6. Change in the output voltage, V_{OUT}, base-emitter voltage V_{BE} of Q_3, and ΔV_{BE} of Q_3 inside first-order BGR irradiated at room temperature as a function of total accumulated dose for samples after (a) X-ray irradiation and (b) 2-MeV proton irradiation.
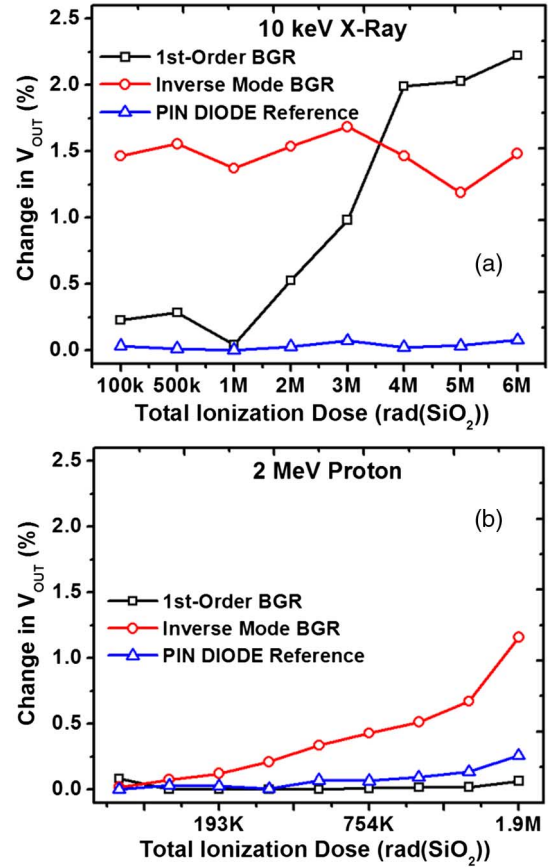
Fig. 7. Voltage reference circuits comparison plotted as functions of total dose and change in V_{OUT} for (a) X-ray irradiation and (b) 2-MeV proton irradiation.

PTAT current, which is then mirrored to the output stage for negative temperature compensation. Therefore, any significant change in the PTAT current affects the BGR output voltage.

The measured change in V_{OUT} for the PIN diode VRC as a function of TID for both X-ray and proton is shown in Fig. 7(a) and (b) (open triangle symbols), respectively. The maximum measured change in V_{OUT} for both irradiation experiments is $\approx 0.25\%$. This percentage change satisfies the majority of applications that require robust bias circuity (e.g., DACs and ADCs). To understand why the PIN diode VRC demonstrates an overall better response to TID in comparison to first-order

and IM BGRs, stand-alone PIN diode device structures of similar size and using the same bias conditions as in the VRCs were irradiated. The measured results at different total doses are illustrated in Fig. 8. Both X-ray [Fig. 8(a)] and proton [Fig. 8(b)] results confirm that the change in diode current for a V_{AC} bias at ≈ 0.8 V is minimal, and thus the impact on the VRC output is insignificant.

The change in V_{OUT} comparison between the three VRCs for both X-ray and proton experiments is shown in Fig. 7(a) and (b), respectively. Since the X-ray source yielded the worst-case VRC performance degradation, the VRCs were characterized

TABLE I
MEASURED *dc* PERFORMANCE COMPARISON OF THE VOLTAGE REFERENCE CIRCUITS FOR X-RAY IRRADIATION

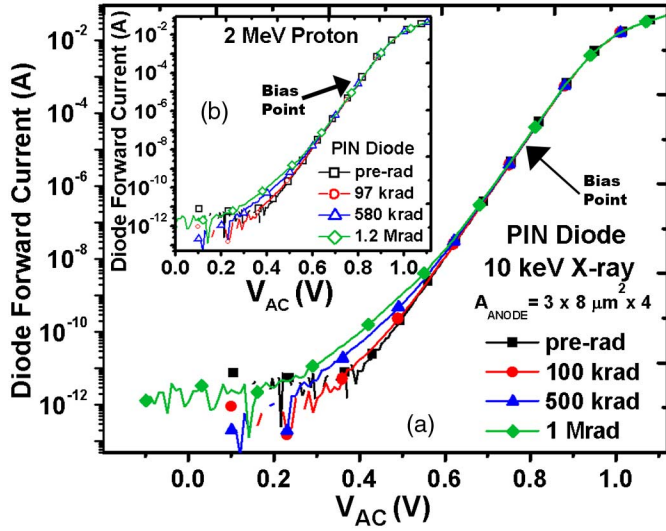| Reference Voltage Circuit	V_{OUT} (V) @ 27 °C			I_{CC} (µA) @ 27°C			Temp. Coefficient (ppm/°C)		
	Simulation	Measured		Simulation	Measured		Measured (-53:127 °C)		
		pre-rad	post-rad*		pre-rad	post-rad*	pre-rad	post-rad*	%Δ
First-order BGR	1.079	1.083	1.008	332	320	565	24	189	155
Inverse-Mode (IM) BGR	1.064	1.061	1.088	319	278	310	43	64	39
PIN Diode	1.858	1.855	1.863	85	69.5	73	67	174	88

Fig. 8. Measured PIN diode transfer characteristics as a function of total accumulated dose for standalone samples (a) after X-ray irradiation and (b) after 2-MeV proton irradiation. The same bias conditions were used for the PIN diodes during irradiation, V_{AC} of ≈ 0.8 V.

before and after X-ray irradiation from $-53\,°C$ to $127\,°C$ at equivalent total dose level of 6 Mrad(SiO$_2$). The measured *dc* performance of the VRCs is summarized in Table I. The results confirm that both proposed RHBD approaches improve the circuit robustness to TID when compared with the non-RHBD first-order BGR. The percentage change of the VRCs TC is also calculated and included in Table I. The TC value is measured in parts per million per degree Celsius (ppm/°C) and is one of the most important specifications for a VRC, since it measures how much the VRC output voltage changes for a given temperature range. According to the values shown in the table, the TC value implies that the IM BGR is more robust to TID exposure than the PIN VRC. However, as previously stated in Section II, unlike the first-order and IM BGRs, the PIN diode VRC does not incorporate any temperature compensation technique. Therefore, when comparing the respective calculated TC values, this fact needs to be taken in consideration. The post-irradiation data present in this table only include X-ray data since it yielded the worst-case VRC performance degradation.

V. SUMMARY

SET and TID experiments were performed on first-order BGR circuits designed in a fourth-generation 90-nm SiGe BiCMOS technology. The results presented here confirm that SiGe-based BGR circuits are sensitive to SET, but the circuits demonstrate minimal degradation to TID exposure. Based on first-order circuit results, circuit-level RHBD techniques using IM SiGe HBTs and a PIN diode VRC as potential RHBD strategies were presented. The extracted FWHM transient duration at the V_{OUT} node for the IM BGRs decrease by approximately three orders of magnitude when compared with the first-order BGR, 600 ns and 0.7 ns, respectively. A decrease in transient peak, transient duration, and collected charge was observed. This occurs because the electrical collector (physical emitter) of the IM SiGe HBTs are electrically isolated from the sensitive subcollector-substrate junction. These results are significant, as it confirms that the proposed IM circuit-level RHBD technique can be used for SET mitigation on this type of an ubiquitous analog circuit without increasing the TID sensitivity.

For the PIN VRC, no transients were observed when 2-D raster scans were performed from laser strikes on diode D_2. Transients were not observed at the V_{OUT} terminal of the PIN diode VRC because 1) charge collection at the anode is minimized because the P+ region (anode) is DT-isolated; the forward-biased diode limits charge separation and reduces charge collection at the sensitive node (source of nFET transistor M_7); and 2) any transients at this sensitive node are potentially filtered out because the large resistance from the PIN diode along with the parasitic capacitances of nFET M_7 and diode M_7 form an *RC* low pass filter. The proposed PIN diode RHBD approach demonstrates a higher degree of immunity to SETs at the circuit level, in comparison to the first proposed RHBD approach that uses IM SiGe HBTs.

The 10-keV X-ray and 2-MeV proton irradiation experiments confirm that both the first-order and IM BGRs have radiation-source dependence. The X-ray source yielded the worst-case changes at the V_{OUT} terminal. At a TID of 6 Mrad(SiO$_2$), the largest observed changes at V_{OUT} are ≈ 2.2%, ≈ 1.5%, < 0.25% for the first-order, the IM BGR, and the PIN diode BGR, respectively. Since the X-ray source yielded the worst-case VRC performance degradation, the

VRCs were characterized over-temperature pre- and post-irradiation [TID of 6 Mrad(SiO$_2$)]. The calculated TC value implies that the IM BGR is more robust than the PIN VRC to TID exposure.

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