Accurate Modeling of Single-Event Transients in a SiGe Voltage Reference Circuit

Kurt A. Moen, *Student Member, IEEE*, Laleh Najafizadeh, *Member, IEEE*, Jung Seungwoo, *Student Member, IEEE*, Ashok Raman, *Member, IEEE*, Marek Turowski, *Senior Member, IEEE*, and John D. Cressler, *Fellow, IEEE*

***Abstract*—Single-event transients (SETs) are modeled in a SiGe voltage reference using compact model and full 3-D mixed-mode TCAD simulations. The effect of bias dependence and circuit loading on device-level transients is examined with regard to the voltage reference circuit. The circuit SET simulation approaches are benchmarked against measured data to assess their effectiveness in accurate modeling of SET in SiGe analog circuits. The mechanisms driving the SET of this voltage reference are then identified for the first time and traced back to the original device transients. These results enable the differences between the simulation results to be explained, providing new insight into best practices for the modeling circuit SET in different circuit topologies and device technologies.**

***Index Terms*—Radiation effects modeling, radiation hardening, silicon-germanium (SiGe) heterojunction bipolar transistor (HBT), single-event transients (SETs), TCAD, voltage reference.**

I. Introduction

MODERN silicon-germanium (SiGe) heterojunction bipolar transistors (HBTs) are well suited for a wide variety of analog, RF and high-speed digital circuits, due to their high-frequency operation, low broadband and 1/f noise, high transconductance per unit area, and compatibility with conventional complementary metal–oxide semiconductor (CMOS) fabrication that enables high levels of integration. Due to its inherent tolerance to multi-$\mathrm{Mrad(SiO_2)}$ total ionizing dose (TID) radiation and improved dc and ac performance at cryogenic temperatures [1], SiGe BiCMOS technology has also emerged as a strong contender for extreme environment applications, such as space-based electronics.

Single-event effects (SEEs) remain an area of concern for space-based SiGe circuits, since sufficient immunity to SEEs is a necessity for any space-qualified electronics platform. In view of this, the inherent susceptibility of SiGe digital logic circuits to single-event upset (SEU) is a concern [2], [3], one that is further compounded by the apparent increase in SEU (proton) sensitivity at cryogenic temperatures [4]. In order to mitigate SEU, a variety of circuit- [2], [5], [6] and device-level hardening techniques [7], [8] have been implemented with minimal impact on system complexity. These radiation-hardening-by-design (RHBD) techniques can be supported considerably by modeling and simulation-at the device level through 3-D physical TCAD simulations of ionizing radiation effects and at the circuit level either through traditional compact modeling or true mixed-mode simulations (compact models + 3-D TCAD). Nevertheless, effective optimization of RHBD techniques can only be performed when there is sufficient fidelity between simulated and measured single-event transients (SETs). The SEE response at the circuit level depends heavily on the circuit topology due to feedback effects, varying device biases, and for certain circuits, dynamic biases that evolve on the same time scale as that of measured device SET. Moreover, the importance of addressing this issue when modeling SET grows as circuit response times scale and become comparable to the duration of the individual transistor transients [9]. Clear guidelines must be established as to which approaches to modeling SET are valid for various conditions (circuit topology, technology node, device geometry, environment, etc.).

With this in mind, we investigate here four different approaches to modeling circuit-level SET, using as a test case a SiGe bandgap reference (BGR) circuit [10] for which measured data have been published [11]. Our goal is to first assess how well the simulation approaches correlate to the measured data, then to illuminate for the first time the underlying circuit SET mechanisms, and, finally, to use these conclusions to explain the differences between the simulation results and illuminate possible pitfalls and best practices for circuit SET modeling. The first three simulation approaches utilize a strictly compact model-based circuit in which injected current transients serve to model the effects of a heavy ion strike. This technique has been successfully used to match simulated transients to measured data in an analog circuit [12], but in this older-generation circuit, the SEE response was several orders of magnitude longer than the single-device response. The differences between the compact model-based approaches lie in the origin of the injected current transients: 1) analytical double exponentials versus 2) 3-D TCAD computed transients for a negative substrate bias versus 3) 3-D TCAD computed transients at the corresponding circuit nodal biases. The fourth approach is to use a full mixed-mode simulation, in which a 3-D physical TCAD model is substituted in place of a compact model and solved simultaneously with the full compact modeled circuit [13].

Section II describes the BGR circuit and experimental results. Section III details the circuit-level simulation approaches and the bias dependence of the HBT transient response as illuminated by 3-D TCAD simulations. The simulated SET response of the voltage reference circuit using each approach is

Manuscript received September 17, 2010; revised November 24, 2010; accepted January 10, 2011. Date of publication March 03, 2011; date of current version June 15, 2011. This work was supported in part by the NASA ETDP SiGe project, in part by AFOSR MURI, and in part by a NASA SBIR.

K. A. Moen, J. Seungwoo, and J. D. Cressler are with the Georgia Institute of Technology, Atlanta, GA 30332 USA (e-mail: kmoen@ece.gatech.edu; jung@gatech.edu; cressler@ece.gatech.edu).

L. Najafizadeh was with the Georgia Institute of Technology, Atlanta, GA 30332 USA. She is now with the National Institutes of Health, Bethesda, MD 20892 USA (e-mail: najafizadehl@mail.nih.gov).

A. Raman and M. Turowski are with the CFD Research Corporation (CFDRC), Huntsville, AL 35805 USA (e-mail: ar2@cfdrc.com; mt@cfdrc.com).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TNS.2011.2107333

0018-9499/$26.00 © 2011 IEEE

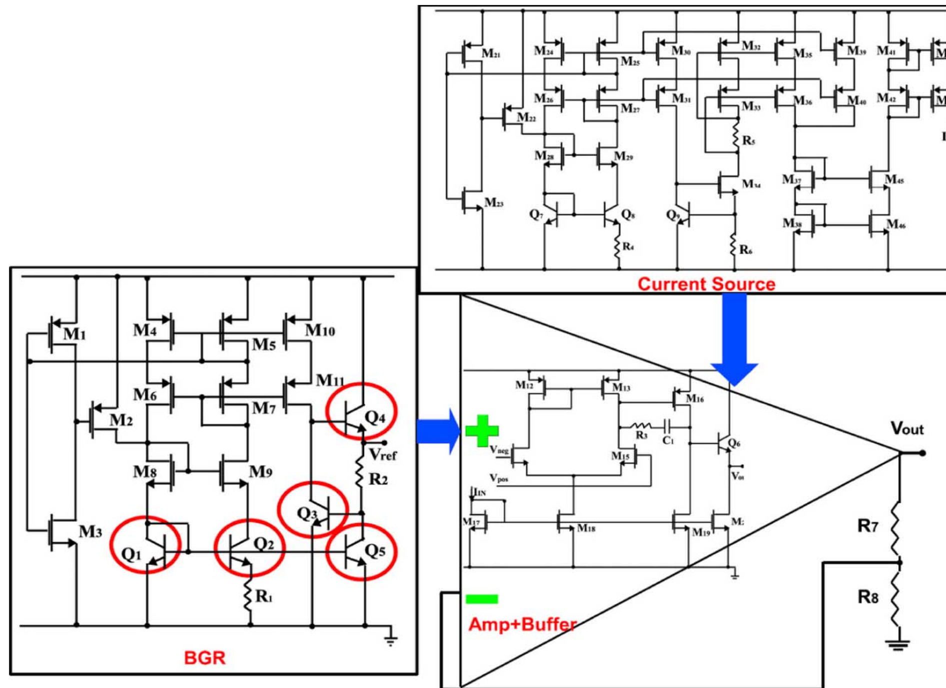

Fig. 1. SiGe voltage reference circuit schematic. The circuit exhibits the greatest sensitivity to transients induced in transistor Q2 [11].

then presented in Section IV and compared to the measured data. The BGR output transient is deconstructed using the mixed-mode simulation results to determine its driving components; having established these mechanisms, we identify the reasons underlying the similarities and differences of the simulation approaches, providing insight for future work on circuit SET in different circuit topologies and device technologies.

II. Background

Experimental data have been reported on laser- and microbeam-induced transients in single devices from first-generation SiGe BiCMOS technology [14]. Recently, measured microbeam-induced transients have also been published for a SiGe precision voltage reference circuit fabricated in this same SiGe technology [11]. Results of these studies show the strong bias dependence of individual HBT transients and the much longer transients at the output of the voltage reference compared to that of the single transistor (~300 ns and ~10 ns, respectively).

The SiGe voltage reference is described in [10] and [11]; its schematic is reproduced in Fig. 1. An exponential, curvature-compensated BGR [10] was used to provide the reference voltage to the positive input of an operational amplifier (opamp) [11]. The opamp is a two-stage amplifier followed by an emitter-follower buffer from which the experimental SETs were measured. The opamp is biased with an on-chip current source. The SiGe BGR circuit is designed to generate an output voltage of 1.17 V at room temperature, and an output voltage of 1.65 V is expected from the regulator. During normal circuit operation, the substrate is grounded and a power supply of 3.3 V is used to bias the circuit. The output voltage of the BGR is defined by the sum of two components: 1) the $\mathrm{V_{BE}}$ of transistor Q3 and 2) the voltage drop across resistor R2, which is determined by the sum of the base current flowing through Q3 and the collector current flowing through Q5.

CFDRC's NanoTCAD tool [15] was used to perform simulations of normally incident emitter-center ion strikes on transistor Q2 ($0.5 \times 2.5\ \mu\mathrm{m}^2$ SiGe HBT), since experimental ion strikes on this transistor produced the largest circuit output transients. In order to model the complex ion track, the SRIM software tool [16] was used to compute an energy-deposition versus depth profile for the 36-MeV oxygen ion used in the microbeam tests, taking into account the back-end-of-line (BEOL) layers present above Q2. This variable linear energy transfer (LET) profile was then imported into NanoTCAD using its automated ion track meshing capability. In the voltage reference circuit, transistor Q2 is biased at $\mathrm{V_B} = 0.74$ V, $\mathrm{V_E} = 0.05$ V, $\mathrm{V_C} = 0.74$ V, with the substrate grounded. The peak of all TCAD ion strikes presented here occurs at 2 ps. The measurement setup and experimental conditions are detailed in [11] and [14].

III. SET Simulation Approaches

A. Compact Model Simulations

The first simulation approach is to inject an analytical double exponential current transient within the Spectre model of the BGR at the terminals of Q2. Analytical current sources have been used extensively for both analog [17] and digital circuits [18] as well as to investigate novel device architectures [8]. This approach is easily implemented and enables a straightforward analysis of the critical LET or collected charge associated with SEE. In addition, the use of an analytical transient avoids convergence issues that can arise with piecewise-linear transient sources based on TCAD or measured transients [19]. The double exponential source used in this paper is calibrated to 3-D TCAD simulations and is illustrated in Fig. 2. In the second approach, a piecewise-linear current source is used to inject the 3-D TCAD-computed transients at the terminals of Q2. In this case, the device terminals are grounded with a substrate bias of −4 V, since bipolar logic is primarily sensitive to strikes on

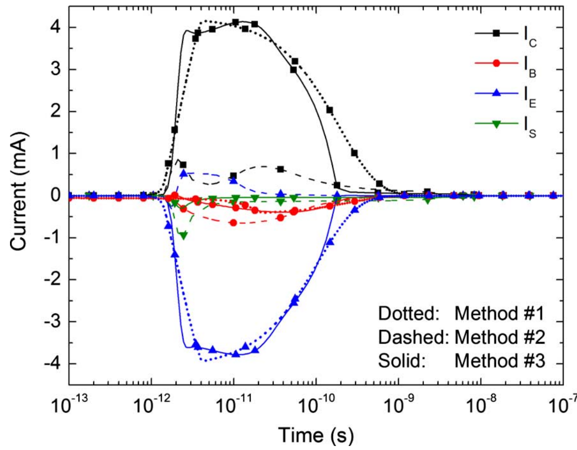

Fig. 2. Comparison of injected device transients from each simulation approach: 1) double exponential, 2) 3-D TCAD SiGe HBT transients at $V_{SX} = -4$ V, and 3) 3-D TCAD transients at Q2 biases. Transients are for a single device not within the circuit.

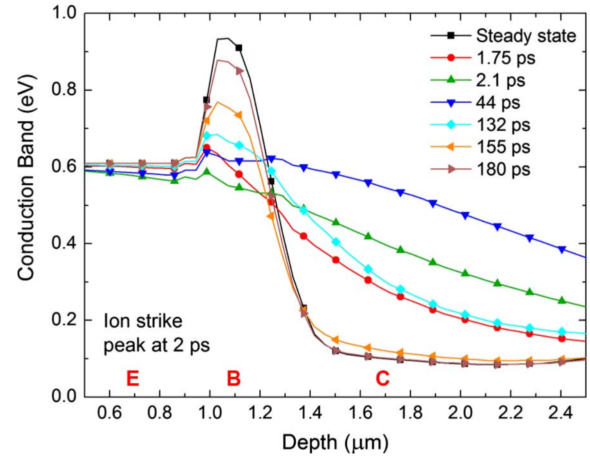

Fig. 3. Time evolution of the conduction band energy within a SiGe HBT during a simulated ion strike, taken from a line probe through the center of the emitter. The ion strike peak occurs at 2 ps, with a Gaussian decay of 250 fs.

the "OFF" transistor due to charge collection at the collector terminal through the collector to substrate junction. This approach was chosen to provide a point of comparison for the bias dependence of the device-level transients as well as a measure of how this bias dependence is reflected at the circuit output. The third simulation approach uses piecewise-linear transients based on TCAD transients, biased in this case at the nodal potentials of Q2. Both sets of TCAD transients are shown in Fig. 2. The primary drawback of these approaches is that they are based on single transistor transients in which there is no loading or feedback from the external circuit [18], [19].

B. Bias Dependence of a SiGe HBT SET

Fig. 2 demonstrates that the SET of a SiGe HBT possesses strong bias dependence. The SET simulated at the nodal biases of Q2 demonstrates greatly increased collector and emitter transients compared to that of the HBT with a negative substrate bias and grounded emitter, base, and collector. Two mechanisms have been proposed to explain the large emitter to collector transient: 1) bipolar action, in which modulation of the base potential induces an increase in forward bipolar current and 2) the ion shunt effect, in which the carrier densities are sufficiently high along the ion track such that the emitter is shorted to the collector by an electron-hole plasma wire, leading to large transient currents for nonzero V_{CE} [20]–[22]. The energy bands in Fig. 3, taken from a line probe through the center of the HBT, show a nearly linear slope from the emitter to collector during the time period of the large emitter to collector current, with slight deviations in the base region due to the presence of the SiGe layer. Furthermore, the electron density profile band during this time period is approximately flat except for minor variations in the region with bandgap grading, consistent with a resistor-like shunt current from emitter to collector. These facts indicate that the ion shunt effect dominates the collector and emitter transients of transistor Q2. The net result of an ion strike on a SiGe HBT biased in the forward active region is an amplification of the SET and a corresponding increase in the total collected charge, highlighting the importance of addressing the impact of transistor bias when investigating SEE in analog/RF circuits.

C. True Mixed-Mode SET Simulation

In contrast to strictly compact model-based approaches, true mixed-mode simulations, as described in [9] and [13], possess the advantage of the 3-D TCAD device being exposed to the dynamic biases present in the circuit throughout the SET, at the cost of increased computational complexity. The compact model-based approaches require an initial TCAD transient simulation for each transistor and bias case of interest (one of which typically completes within four hours), followed by circuit transient simulations of minimal duration. In contrast, a single mixed-mode transient simulation requires no initial TCAD transient simulation and typically completes within 10–12 h. Computing the TCAD solution within a circuit enables mixed-mode simulations to account for feedback and loading from the external circuit that can, in principle, alter the device transient currents as they evolve over time. The mixed-mode simulations in this paper were performed using CFDRC's *MixCad* tool (3-D NanoTCAD interface to Cadence Spectre) [13] and a calibrated 3-D TCAD model of a first-generation SiGe HBT. Whereas mixed-mode studies, such as [23], are limited to basic SPICE passives and compact models, the unique interface between NanoTCAD and Spectre allows this mixed-mode tool to be used directly with the compact models included in commercial process design kits. Thus, the mixed-mode simulations presented here entail a 3-D TCAD device operating within the final circuit design as submitted for fabrication, including extracted layout parasitics.

Fig. 4 illustrates the difference in the transient currents at the HBT terminals for a 3-D TCAD simulation at steady-state circuit biases (Method #3 in Fig. 2) and for a TCAD device within a mixed-mode circuit simulation. The magnitude of the mixed-mode emitter and collector transients is significantly reduced, leading to a much lower collected charge (0.49 pC versus 0.74 pC at the collector); thus, the current injection approach overestimates the SET at the device level within this particular circuit. Given the strong bias dependence of SET in the SiGe HBT, along with the widely varying impedances to which devices in analog/RF circuits are exposed, this issue will be heavily dependent on the circuit topology in question. In this case, the emitter transient current causes the emitter voltage to rise due

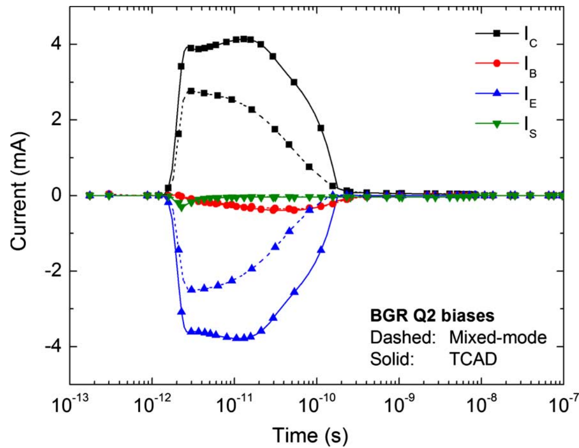

Fig. 4. Comparison of device terminal transients computed from a 3-D TCAD simulation and from within the full 3-D mixed-mode circuit simulation.

to the voltage drop across R1, whereas the collector transient current causes the collector voltage to drop, thus reducing V_{CE} and limiting the shunt current between the emitter and collector.

IV. SiGe Voltage Reference Simulations

A. Circuit-Level Transients

In order to provide a basis for comparing the simulated SET to that reported in [11], the entire measurement path was modeled. Starting from the circuit output, the modeled elements include the bond pad capacitance, bond wire inductance, distributed coaxial transmission line, as well as bias tee and oscilloscope resistive and capacitive loads. A representative diagram of these circuit elements is given in [24].

Figs. 5 and 6 show the simulated transients at the outputs of the BGR and the regulator circuits. The duration of the BGR output transient increases by an order of magnitude relative to that of the single transistor (from ~10 ns to ~100 ns), agreeing with the lengthening of transients in circuits versus individual devices that has been observed experimentally [11]. The transient at the output of the voltage regulator likewise increases in duration by nearly a factor of two, approaching the duration of the measured voltage reference transient. This transient lengthening is consistent across all simulation approaches, indicating that the transient lengthening is driven by the parasitics of the circuit as the signal propagates to the output.

Fig. 7 shows the simulated transients as they would be measured by the oscilloscope, overlaid upon an actual measured transient from a 36 MeV oxygen ion strike, taken from Location 1 of [11], a representative emitter-center strike from Q2. The bias tee present at the oscilloscope terminal removes the dc bias of Fig. 6. The first peak of the mixed-mode result correlates well with the data and its second peak qualitatively follows the shape of the measured transient. As expected from the overestimated transients in the single transistor simulations of Fig. 4, Method #3 (fixed circuit biases) overshoots the mixed-mode transient at the oscilloscope, further exceeding the measured data. Method #1 produces a similar result, since its double exponential input transients are calibrated to the 3-D TCAD transients of Method #3. Despite the large difference in its device-level transients, Method #2 produces a comparable transient at the oscilloscope. Although the mixed-mode simulation demonstrates the closest

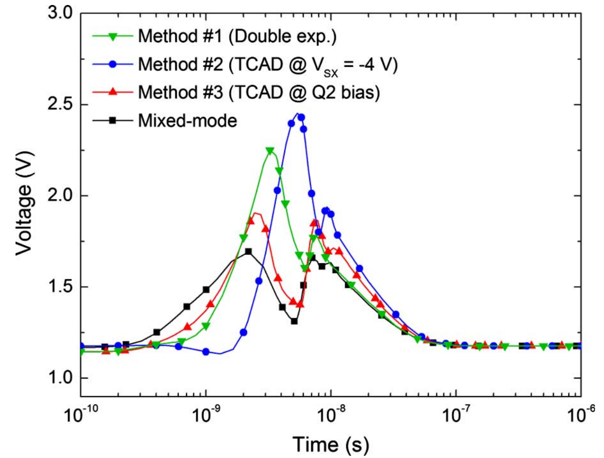

Fig. 5. Comparison of circuit transients at the BGR output as simulated according to the different approaches.

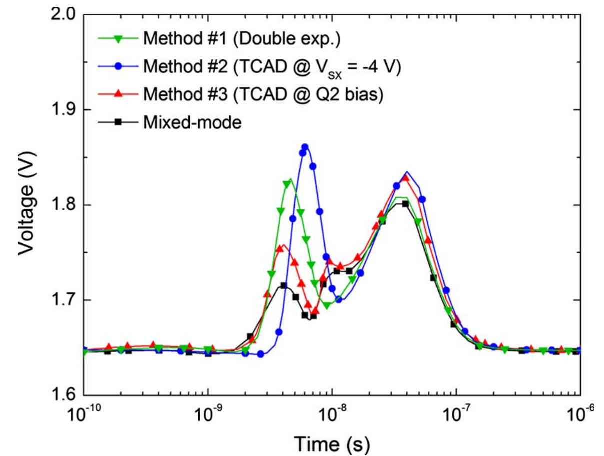

Fig. 6. Comparison of circuit transients at the regulator output as simulated according to the different approaches.

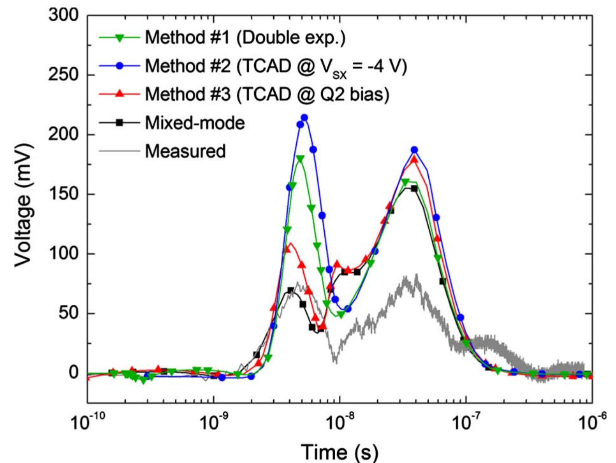

Fig. 7. Comparison of simulated and measured transients at the oscilloscope input. The time scales of the simulated transients have been shifted to align with the measured transient.

agreement to the magnitude and temporal structure of the measured transient, all four approaches give similar qualitative insights into the circuit transient response.

B. Analysis of BGR Output Transient

The factors that drive the temporal shape of the BGR output transient can be identified by carefully tracing the current tran-

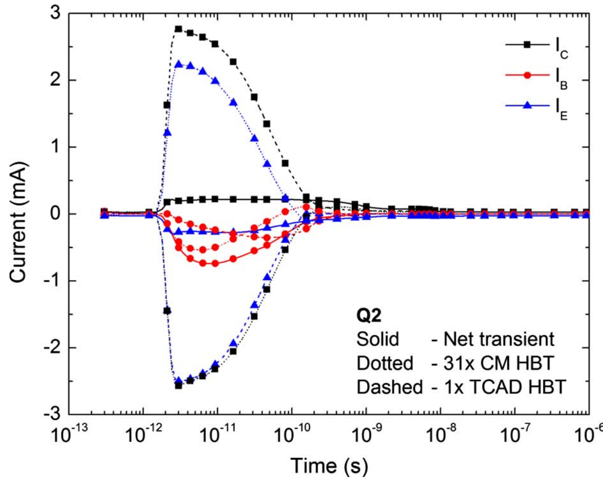

Fig. 8. Mixed-mode transient currents at Q2: currents at the single irradiated TCAD transistor (dashed), currents at the 31 parallel compact model HBTs and net transient currents to the remainder of the circuit from the 32x array (solid).

sients from their origin at Q2 to the circuit output. Since the four approaches give similar qualitative results, we will analyze in detail the mixed-mode simulation. The first important fact is that Q2 is composed of an array of 32 HBTs wired in parallel; in both experiment and simulation, a given SET event is recorded when only one of these 32 HBTs is subject to a heavy ion strike. Charge sharing between adjacent HBTs is negligible, indicated by the fact that the sensitive areas of each HBT in Q2 as shown in [11] do not overlap. Moreover, 3-D TCAD simulations encompassing two HBTs spaced apart as in the physical layout demonstrate that for an ion strike to the emitter-center of one HBT, the peak transient collector current on the adjacent HBT is three orders of magnitude less than that of the irradiated device; this is also confirmed in [25]. The mixed-mode circuit simulation results show that a significant portion of the collector and emitter current originating in the irradiated HBT is absorbed by the 31 parallel compact model HBTs. Fig. 8 shows the ion-induced transients from the 3-D TCAD HBT along with the total current transients at the 31 parallel HBTs. The resulting net transients from the Q2 array are significantly different from the irradiated device transients, with reduced peak collector and emitter currents and increased negative base current. Referring to the schematic in Fig. 1, the base of Q2 is shared with transistors Q1 and Q5. Consequently, the net base current flowing from Q2 is divided between Q1 and Q5.

Fig. 9 shows the terminal current transients for Q5. The initial rising base transient is capacitively coupled to the emitter, but bipolar conduction begins to dominate due to modulation of the base potential for times greater than approximately 30 ps. Although the Q5 collector current transient will lead to modulation of the BGR output voltage through the voltage drop across R2, the influence of Q3 must be considered, since the base of Q3 is tied to the collector of Q5. Fig. 10 plots the terminal current transients for Q3, in which the initial negative base and positive emitter currents show that capacitive coupling of the base and emitter of Q5 supplies a portion of the collector current of Q3. The influence of the resistive drop due to current in the output branch can be estimated by summing the Q3 base and Q5 collector transients, as plotted in Fig. 11. Three peaks emerge in the sum of the two currents: near 100 ps, near 2 ns, and near 10

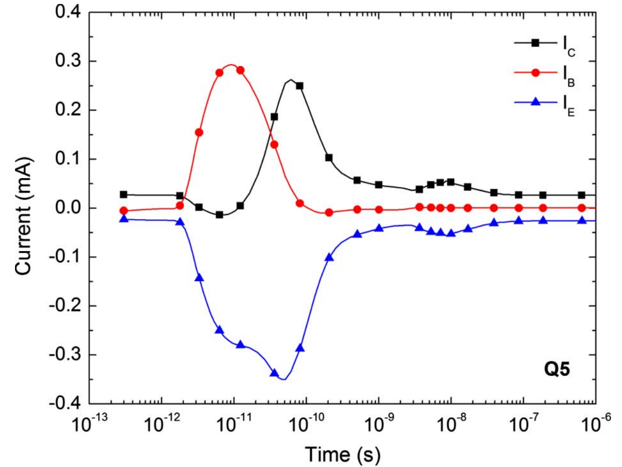

Fig. 9. Mixed-mode current transients at the terminals of transistor Q5.

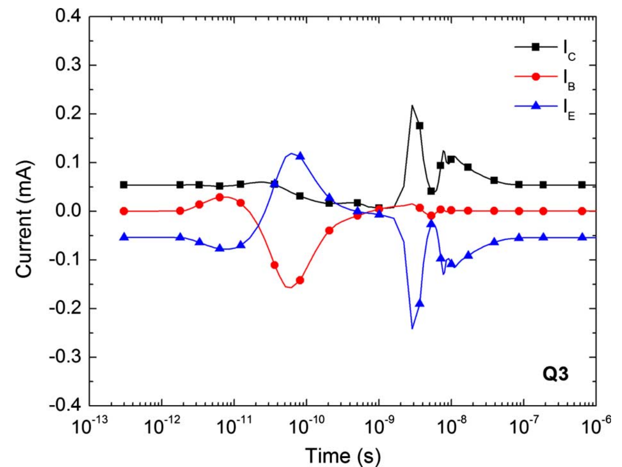

Fig. 10. Mixed-mode current transients at the terminals of transistor Q3.

ns. The first and third peaks are driven by the collector current of Q5, with the second peak driven by the base current of Q3. The output voltage then increases according to the total transient current through R2. Due to the distributed resistance and parasitic capacitance of R2, the high-frequency components of the current transient are transformed to lower frequencies as it propagates through the resistance network, as illustrated in Fig. 12. Consequently, the first and second peaks of the summed current in Fig. 11 are conflated together in the output transient.

Whereas the initial rise in the output voltage originates with the increasing Q5 collector current, the subsequent output response is determined by a damped feedback loop involving Q3, Q4, Q5, R2, and M11. As the output voltage rises due to the current transient through R2, the voltage at the drain of M11 also increases due to the emitter follower Q4 until M11 is ultimately driven into the linear regime near 1 ns. This process is illustrated in Fig. 13, which plots key transistor biases for the duration of the SET. The simulation results show that the source voltage of M11 rises slightly in order to compensate for the rising drain voltage, but is limited by the cascoded M10. The V_{SG} of M11 also increases slightly as M7 conducts more current to support the collector transient of Q2 as it propagates through M9. As M11 is pushed out of saturation, its drain current decreases significantly, reducing the base current that flows into Q4; this forces a reduction of the emitter current of Q4, followed by a decrease in the output voltage as less current flows

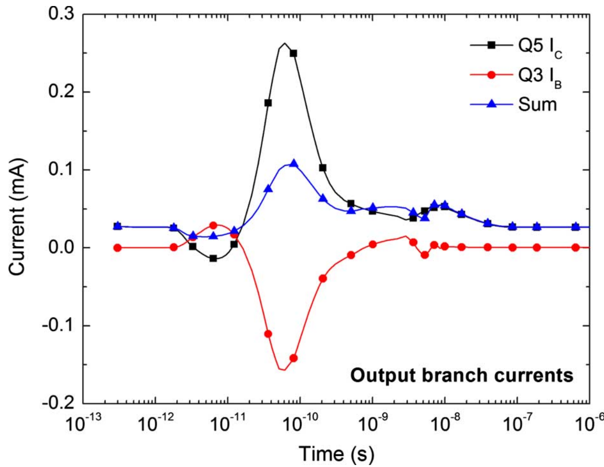

Fig. 11. Mixed-mode current transients that contribute to the BGR output voltage through the resistive drop across R2.

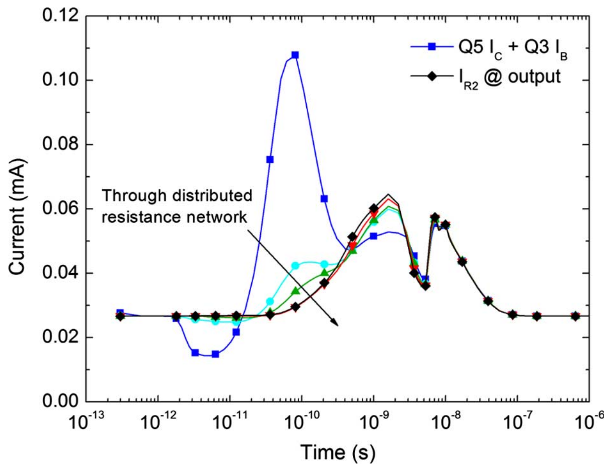

Fig. 12. Transformation of current transient as it flows through resistor R2, a polysilicon resistor modeled as a distributed network of resistors and parasitic capacitors.

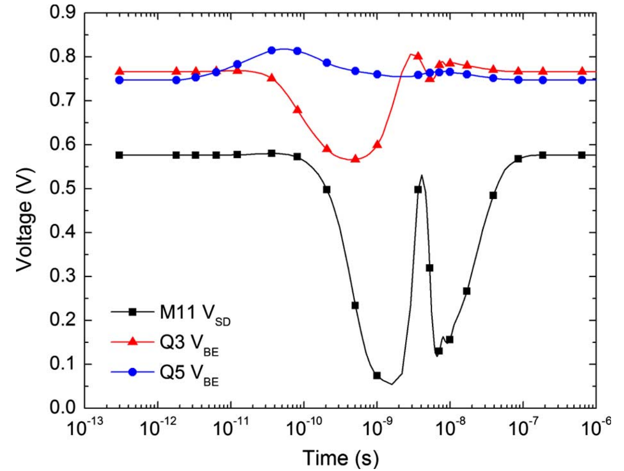

Fig. 13. Mixed-mode voltage bias transients for transistors M11, Q3, and Q5.

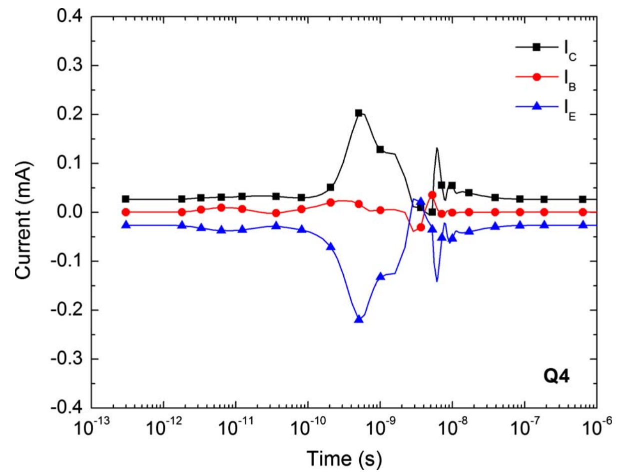

Fig. 14. Mixed-mode current transients at the terminals of transistor Q4.

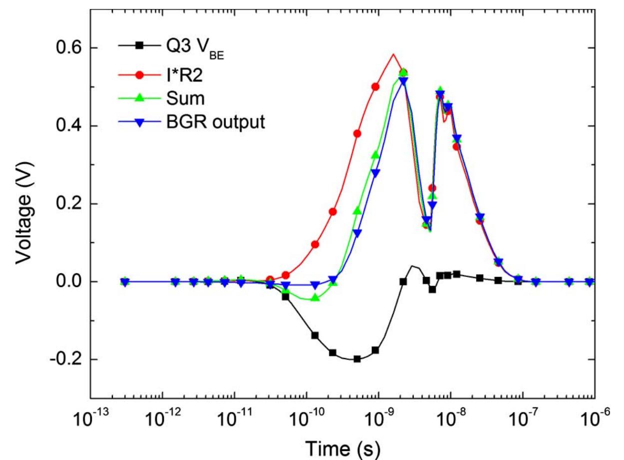

Fig. 15. Mixed-mode BGR output transient along with its key components: the resistive drop across R2 and the V_{BE} across Q3. The dc offset of each curve has been removed to highlight the contributions of each component to the overall SET.

through R2. However, as soon as the output voltage begins to decrease, M11 re-enters saturation and experiences a sharp increase in its drain current around 3 ns. The collector and base currents of Q3 increase accordingly and the emitter current of Q4 increases sharply as more current flows into its base, causing the Q5 collector current to increase. Together, these currents cause the output voltage to rise again until M11 once again approaches linear operation. The feedback from the drain current of M11 is less severe at this point, since the current flowing through R2 peaks at a lower magnitude. The circuit output transient is then controlled by decreasing oscillations of the Q3 base current and a steady decrease of the Q5 collector current.

Since the BGR output voltage is the sum of the V_{BE} across Q3 in addition to the voltage drop across R2, the transient response of V_{BE} must also be considered. Fig. 15 plots the BGR output transient along with these components, with the dc offset removed in order to identify the contributions of each component. This plot reveals that the output voltage transient is defined primarily by the current component, as the V_{BE} transient is significantly smaller than the voltage drop across R2. The V_{BE} transient corresponds to the shape of the Q3 base current and serves primarily to retard the rising edge of the output transient. In Fig. 15, the current and voltage components are summed together to demonstrate a close match to the simulated voltage transient at the output, indicating that it is valid to assume that the current component of the output transient can be represented by current simulated at the top of R2 times the total resistance of R2.

In summary, the initial rising output voltage results from a rising Q5 collector current combined with a subsequent

increase in the Q3 base current. The sharp roll off and subsequent increase in the output voltage are caused by a feedback loop: the roll-off occurs when M11 enters linear operation, lessening the Q4 base current and reducing its emitter current that flows through R2; the decreasing output voltage enables M11 to re-enter saturation, resulting in a large signal increase in its drain current, which causes Q3 and Q4 directly and Q5 indirectly to conduct more current. The output voltage then peaks a second time, followed by decreasing oscillations due to the Q3 base current and a steady decrease due to the Q5 collector current.

C. Comparison of Simulation Approaches

Having decomposed the BGR output transient, the origin of the similarities and differences between simulation approaches can be identified. The results show that the analog circuit output is primarily sensitive to the base transient on Q2, unlike traditional digital circuits; as such, although accounting for the actual circuit biases yields the most accurate results, a qualitative match is still achieved by Method #2 since it has a comparable base transient. On the other hand, the reduction in collector and emitter transients shown in Fig. 4 cannot explain the difference in the output transients between the mixed-mode simulation and Method #3. The chief deviation between the mixed-mode and current injection results is that the negative base transient is much larger in the current injection simulations. Figs. 16 and 17 show the injected and net transients at Q2 for Methods #1 and #3, respectively. The larger base current results in a larger Q5 collector current, thus increasing the base current drawn from Q3 and together causing a much larger initial voltage peak at the BGR output. Subsequently, the larger output transient forces M11 further out of saturation than in the mixed-mode simulation. Since a larger initial Q5 collector transient pulls current from R2 and the base terminal of Q3, there is only a marginal increase in the base transient of Q3 and its V_{BE}. Consequently, each simulation approach shows a similar reduction in the output voltage due to the feedback loop. Since the first output peak is a direct result of current flowing from the Q2, the differences are striking for different base transient magnitudes. However, the second output voltage peak is only affected indirectly by the base transient current, since it is a determined by the feedback loop of Q3, Q4, Q5, and M11. As a result, the current injection approaches still estimate a larger second peak of the output voltage than the mixed-mode simulation, but the differences are less prominent. Since the base transient of Method #1 subsides before that of Method #3, its simulated output is closer to that of the mixed-mode simulation at the second peak. Nevertheless, all four approaches overestimate the second peak of the measured output voltage. This is possibly due to the fact that some of the underlying 3-D TCAD simulations of an HBT ion strike overestimate the measured SET duration for a single device [24]. Considering Fig. 9, if more transient base current is forced into Q5 for a longer period of time, a larger forward bipolar current will be induced, leading to a stronger feedback mechanism and larger BGR output transient. Discrepancies at the device level will likely be reflected at the circuit level if they are due to inaccuracies in the physical models. Further work needs to be performed to reconcile all simulation to data discrepancies at the device level and to assess their impact on circuit-level SET simulations and this is in progress.

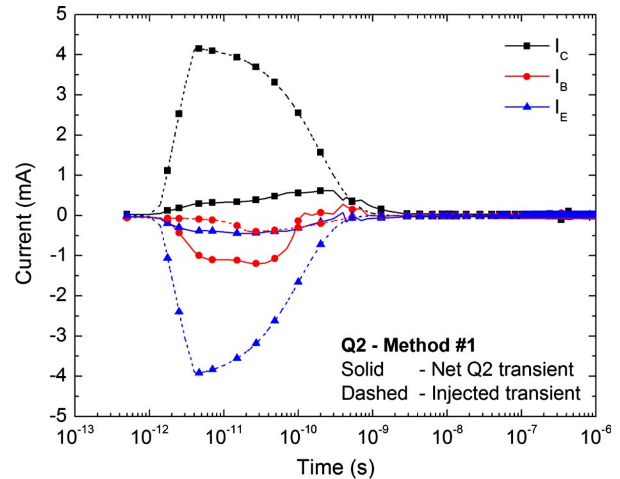

Fig. 16. Transient currents at Q2 using Method #1: injected current transients (dashed) and net transient currents seen by the remainder of the circuit (solid).

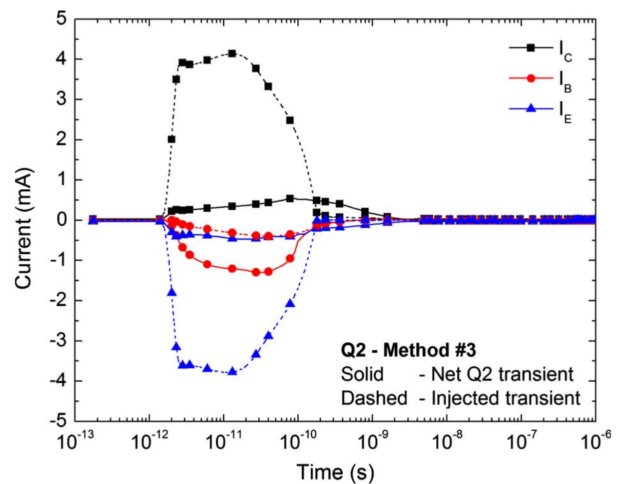

Fig. 17. Transient currents at Q2 using Method #3: injected current transients (dashed) and net transient currents seen by the remainder of the circuit (solid).

V. SUMMARY

Four different approaches to modeling SETs in circuits have been applied to a precision SiGe voltage reference circuit. The importance of modeling the bias dependence of the single device transient was shown by comparing 3-D TCAD transients of a SiGe HBT at negative substrate bias with those of a SiGe HBT mirroring the biases of transistor Q2 from the BGR. The ion shunt effect was shown to be the driving factor for the large collector to emitter transients from Q2. The primary limitation of current injection approaches is that they do not account for the loading of the device terminals that shifts the terminal biases throughout the duration of the SET, as evidenced by the difference between the HBT terminal transients simulated using TCAD alone and those simulated within a full mixed-mode circuit simulation (Fig. 4).

With this knowledge of both the device-level response and circuit loading, the effectiveness of each modeling approach was tested at the circuit level against measured transients in a SiGe

voltage reference. Although the mixed-mode simulation is marginally closer to the measured transient, all three current injection approaches also capture the basic shape of the circuit SET. The reasons behind this were illuminated by a detailed analysis of the transient response of the circuit, which enabled the mechanisms that drive the major components of the circuit SET to be traced back to the original device transients at Q2, revealing that the base transient of Q2 is the driving force behind the circuit SET. For this particular BGR circuit, current injection approaches provide similar qualitative insights, since in this case, the circuit loading and bias conditions strongly affect the collector and emitter transients, but only marginally affect the base transient that drives the circuit SET. However, this result is entirely dependent on the circuit topology and must be examined for other analog and RF circuits in which loading effects may influence the critical device-level transients (e.g., in dynamic circuits such as voltage-controlled oscillators). Loading effects need to be examined at more aggressive scaling nodes (e.g., 130 nm) where circuit response times are comparable to single-device SET durations. Moreover, for novel device structures, such as [8], for which no calibrated compact model presently exists, SET can be realistically modeled only by full mixed-mode simulation.

ACKNOWLEDGMENT

The authors would like to thank G. Niu for helpful discussions.

REFERENCES

[1] J. D. Cressler, "On the potential of SiGe HBTs for extreme environment electronics," *Proc. IEEE*, vol. 93, no. 9, pp. 1559–1582, Sep. 2005.

[2] P. W. Marshall, M. A. Carts, A. Campbell, D. McMorrow, S. Buchner, R. Stewart, B. Randall, B. Gilbert, and R. A. Reed, "Single event effects in circuit-hardened SiGe HBTs at gigabit per second data rates," *IEEE Trans. Nucl. Sci.*, vol. 47, no. 6, pt. 3, pp. 2669–2674, Dec. 2000.

[3] R. A. Reed, P. W. Marshall, J. C. Pickel, M. A. Carts, B. Fodness, G. Niu, K. Fritz, G. Vizkelethy, P. E. Dodd, T. Irwin, J. D. Cressler, R. Krithivasan, P. Riggs, J. Prairie, B. Randall, B. Gilbert, and K. A. LaBel, "Heavy-ion broad-beam and microprobe studies of single-event upsets in 0.20-μm SiGe heterojunction bipolar transistors and circuits," *IEEE Trans. Nucl. Sci.*, vol. 50, no. 6, pt. 1, pp. 2184–2190, Dec. 2003.

[4] A. K. Sutton, K. Moen, J. D. Cressler, M. A. Carts, P. W. Marshall, J. A. Pellish, V. Ramachandran, R. A. Reed, M. L. Alles, and G. Niu, "Proton-induced SEU in SiGe digital logic at cryogenic temperatures," *Solid State Electron.*, vol. 52, no. 10, pp. 1652–1659, 2008.

[5] G. Niu, R. Krithivasan, J. D. Cressler, P. Marshall, C. Marshall, R. Reed, and D. L. Harame, "Modeling of single event effects in circuit-hardened high-speed SiGe HBT logic," *IEEE Trans. Nucl. Sci.*, vol. 48, no. 6, pt. 1, pp. 1849–1854, Dec. 2001.

[6] R. Krithivasan, G. Niu, J. D. Cressler, S. M. Currie, K. E. Fritz, R. A. Reed, P. W. Marshall, P. A. Riggs, B. A. Randall, and B. Gilbert, "An SEU hardening approach for high-speed SiGe HBT digital logic," *IEEE Trans. Nucl. Sci.*, vol. 50, no. 6, pp. 1849–1854, Dec. 2003.

[7] A. K. Sutton, M. Bellini, J. D. Cressler, J. A. Pellish, R. A. Reed, P. W. Marshall, G. Niu, G. Vizkelethy, M. Turowski, and A. Raman, "An evaluation of transistor-layout RHBD techniques for SEE mitigation in SiGe HBTs," *IEEE Trans. Nucl. Sci.*, vol. 54, no. 6, pt. 1, pp. 2044–2052, Dec. 2007.

[8] S. Phillips, T. Thrivikraman, A. Appaswamy, A. K. Sutton, J. D. Cressler, G. Vizkelethy, P. Dodd, and R. A. Reed, "A novel device architecture for SEU mitigation: The inverse-mode cascode SiGe HBT," *IEEE Trans. Nucl. Sci.*, vol. 56, no. 6, pp. 3393–3401, Dec. 2009.

[9] M. Turowski, A. Raman, and G. Jablonski, "Mixed-mode simulation and analysis of digital single event transients in fast CMOS ICs," in *Proc. Int. Conf. Mixed Design of Integrated Circuits and Systems*, 2007, pp. 433–438.

[10] L. Najafizadeh, A. K. Sutton, R. M. Diestelhorst, M. Bellini, B. Jun, J. D. Cressler, P. W. Marshall, and C. J. Marshall, "A comparison of the effects of X-ray and proton irradiation on the performance of SiGe precision voltage references," *IEEE Trans. Nucl. Sci.*, vol. 54, no. 6, pt. 1, pp. 2238–2244, Dec. 2007.

[11] L. Najafizadeh, S. D. Phillips, K. A. Moen, R. M. Diestelhorst, M. Bellini, P. K. Saha, J. D. Cressler, G. Vizkelethy, M. Turowski, A. Raman, and P. W. Marshall, "Single event transient response of SiGe voltage references and its impact on the performance of analog and mixed-signal circuits," *IEEE Trans. Nucl. Sci.*, vol. 56, no. 6, pp. 3469–3476, Dec. 2009.

[12] P. Adell, R. D. Schrimpf, H. J. Barnaby, R. Marec, C. Chatry, P. Calvel, C. Barillot, and O. Mion, "Analysis of single-event transients in analog circuits," *IEEE Trans. Nucl. Sci.*, vol. 47, no. 6, pp. 2616–2623, Dec. 2000.

[13] M. Turowski, A. Raman, and A. Fedoseyev, "Mixed-mode simulation of single event upsets in modern SiGe BiCMOS mixed-signal circuits," in *Proc. Int. Conf. Mixed Design of Integrated Circuits and Systems*, 2009, pp. 462–467.

[14] J. A. Pellish, R. A. Reed, D. McMorrow, G. Vizkelethy, V. Ferlet-Cavrois, J. Baggio, P. Paillet, O. Duhamel, K. A. Moen, S. D. Phillips, R. M. Diestelhorst, J. D. Cressler, A. K. Sutton, A. Raman, M. Turowski, P. E. Dodd, M. L. Alles, R. D. Schrimpf, P. W. Marshall, and K. A. LaBel, "Heavy ion microbeam- and broadbeam-induced transients in SiGe HBTs," *IEEE Trans. Nucl. Sci.*, vol. 56, no. 6, pp. 3078–3084, Dec. 2009.

[15] CFD Research Corp., NanoTCAD Software. ver. 2009, Huntsville, AL.

[16] SRIM: The Stopping and Range of Ions in Matter. [Online]. Available: http://www.srim.org/

[17] R. Pease, "Modeling single event transients in bipolar linear circuits," *IEEE Trans. Nucl. Sci.*, vol. 55, no. 4, pt. 1, pp. 1879–1890, Aug. 2008.

[18] D. Munteanu and J.-L. Autran, "Modeling and simulation of single-event effects in digital devices and ICs," *IEEE Trans. Nucl. Sci.*, vol. 55, no. 4, pp. 1854–1878, Aug. 2008.

[19] J. S. Kauppila, A. L. Sternberg, M. L. Alles, A. M. Francis, J. Holmes, O. A. Amusan, and L. W. Massengill, "A bias-dependent single-event compact model implemented into BSIM4 and a 90 nm CMOS process design kit," *IEEE Trans. Nucl. Sci.*, vol. 56, no. 6, pt. 1, pp. 3152–3157, Dec. 2009.

[20] J. R. Hauser, S. E. Diehl-Nagle, A. R. Knudson, and A. B. Campbell, "Ion track shunt effects in multi-junction structures," *IEEE Trans. Nucl. Sci.*, vol. NS-32, no. 6, pp. 4115–4121, Dec. 1985.

[21] A. R. Knudson, A. B. Campbell, J. R. Hauser, M. Jessee, W. J. Stapor, and P. Shapiro, "Charge transport by the ion shunt effect," *IEEE Trans. Nucl. Sci.*, vol. 33, no. 6, pt. 1, pp. 1560–1564, Dec. 1986.

[22] A. R. Knudson and A. B. Campbell, "Charge collection in bipolar transistors," *IEEE Trans. Nucl. Sci.*, vol. 34, no. 6, pp. 1246–1250, Dec. 1987.

[23] X. Wei, T. Zhang, G. Niu, M. Varadharajaperumal, J. D. Cressler, and P. W. Marshall, "3-D mixed-mode simulation of single event transients in SiGe HBT emitter followers and resultant hardening guidelines," *IEEE Trans. Nucl. Sci.*, vol. 55, no. 6, pp. 3360–3366, Dec. 2008.

[24] M. Turowski, J. A. Pellish, K. A. Moen, A. Raman, J. D. Cressler, R. A. Reed, and G. Niu, "Reconciling 3-D mixed-mode simulations and measured single-event transients in SiGe HBTs," *IEEE Trans. Nucl. Sci.*, vol. 57, no. 6, pp. 3342–3348, Dec. 2010.

[25] G. Niu, J. D. Cressler, M. Shoga, K. Jobe, P. Chu, and D. L. Harame, "Simulation of SEE-induced charge collection in UHV/CVD SiGe HBTs," *IEEE Trans. Nucl. Sci.*, vol. 47, no. 6, pt. 3, pp. 2682–2689, Dec. 2000.