A Multi-Piecewise Curvature-Corrected Technique for Bandgap Reference Circuits

Yi Huang*, Chun Cheung†, and Laleh Najafizadeh*
*Department of Electrical and Computer Engineering, Rutgers University, Piscataway, NJ 08854
† Intersil Corporation, 440 U.S. Hwy 22 E, Suite 100, Bridgewater, NJ 08807
E-mail: yhuang85@eden.rutgers.edu, laleh.najafizadeh@rutgers.edu

Abstract—A systematic design methodology utilizing piecewise curvature correction technique for the purpose of improving the temperature coefficient of bandgap references (BGRs) is presented in this paper. It is shown that the temperature dependency of the drain current of a MOSFET transistor depends on the transistor’s operating region. Using this property, a multi-piecewise compensation technique over wide temperature range is achieved by controlling the operating region of MOSFETs through their gate-source voltages. The technique offers several advantages including simplicity, and providing the designers with flexibility to employ a combination of piecewise currents to achieve maximum temperature stability over the desired temperature range. To demonstrate the capability of this approach, the technique is used to effectively reduce the temperature coefficient of a first-order BGR circuit.

Keywords-BiCMOS, Bandgap Voltage References, Curvature Compensation Techniques, Subthreshold Operation.

I. INTRODUCTION

Bandgap references (BGRs) are important building blocks in many analog and mixed-signal circuits including voltage regulators and data converters. The precision of the output voltage or current provided by BGRs plays a key role in the overall performance of the systems. Conventional BGR circuits generally utilize the first-order temperature compensation of a complementary to absolute temperature (CTAT) voltage/current with a proportional to absolute temperature (PTAT) voltage/current [1]. Due to the existence of high-order temperature-dependent terms in CTAT/PTAT parameters, a complete compensation cannot be achieved. To address this issue, several compensation solutions have been proposed to improve the temperature stability of the BGR circuits including [2]-[9].

One of the proposed compensation solutions is the piecewise curvature-corrected technique in which a nonlinear component is used for the compensation [4]-[8]. Different ways for the realization of this technique have been suggested. For example, in [4], the nonlinear component is produced by the subtraction of PTAT and CTAT currents, and is added in the circuit during the higher temperature range when the PTAT component becomes the dominant term, while in [7] a logarithmic current is included during the high temperature range to the output of an exponentially compensated BGR [3] to achieve further temperature stability.

Two common approaches can be observed in all the existing piecewise curvature-corrected techniques: 1) the inclusion of the nonlinear term is done only during a specific temperature range (higher part), and 2) the generated nonlinear term is designed to increase with temperature. If the nonlinear terms can be included properly in the lower temperature regions, the temperature drift of the circuit will be further reduced. The proper inclusion of the nonlinear terms across all temperature ranges mandates the realization of nonlinear currents, that depending on the deviation of output voltage from the nominal value, either decrease or increase with temperature. With the motivation to address these issues, a systematic piecewise curvature-corrected compensation technique is proposed in this paper. The already available PTAT and CTAT currents in the uncompensated BGR circuit are utilized to control the gate terminal of a MOSFET (and hence, its operating region) to generate proper piecewise currents over wide temperature range. The compensation technique can be easily realized, and provides the designer with several options to choose to maximize temperature stability.

This paper is organized as follows: in Section II an analysis of MOSFETs operating in different regions is given. The proposed piecewise compensation approach is described in Section III. Design considerations and an example are presented in Section IV and V, respectively and the conclusion is given in Section VI.

II. BASIC CONCEPTS

It is well known that in an NMOS transistor, when the gate-source voltage ($V_{GS}$) is larger than its threshold voltage ($V_{TH}$), the drain current ($I_D$) is expressed as [1]:

$$I_D = \begin{cases} 
\frac{\mu C_{ox} W}{L} (V_{GS} - V_{TH})^2 & \text{(Saturation)} \\
\frac{\mu C_{ox} W}{L} [(V_{GS} - V_{TH}) V_{DS} - \frac{V_{DS}^2}{2}] & \text{(Triode)}
\end{cases}$$

(1)

where $V_{DS}$ is the drain-source voltage, $\mu$ is the electron mobility, $C_{OX}$ is the gate capacitance per unit area, and $\frac{W}{L}$ is the channel's aspect ratio. In both conditions of (1), $\mu$ and $V_{TH}$ are the temperature dependent parameters. In deep triode region, where $V_{DS} << 2(V_{GS} - V_{TH})$, the drain current can be estimated to be

$$I_D = \frac{\mu C_{ox} W}{L} (V_{GS} - V_{TH}) V_{DS}.$$ 

(2)

The temperature dependency of $\mu$ is described as [10]

$$\mu = \mu_0 \left(\frac{T}{T_0}\right)^{-m}.$$ 

(3)

In (3), $\mu_0$ is the mobility at the reference temperature $T_0$, and $m$ is a positive constant ($\approx 2.3$) [10]. The threshold voltage
For cases 1-c and 1-d, the rate of change in temperature is below subthreshold (deep triode or saturation) region, and as soon as whether \( V_{GS} \) is increasing (cases I-a and I-c) or decreasing (cases I-b and I-d) function of temperature, how the region of operation of the transistor changes with temperature. For example, in case 1-a (1-b), when the operating temperature is above \( T_{CRITICAL} \), the transistor is operating in the subthreshold (deep triode or saturation) region, and as soon as the operating temperature is above \( T_{CRITICAL} \), the transistor is switching into the triode or saturation (subthreshold) region. For cases 1-c and 1-d, the rate of change in \( V_{GS} \) is such that the transistor stays below \( V_{TH} \) over the desired temperature range, and therefore, the transistor will stay in the subthreshold region. Note that in all these cases, it is not necessary for the gate-source voltage to maintain a linear relationship with temperature.

### III. Proposed Compensation Technique

Without loss of generality, for the derivation of equations we will consider NMOS transistors, but the discussion can be applied in a similar way to PMOS transistors as well. Since the aim of the proposed idea is to generate nonlinear currents through applying a temperature dependent voltage to the gate terminal, we first study the temperature behavior of the drain current in different operating regions.

#### A. Temperature Behavior of \( I_D \)

In the following analysis, we assume the temperature dependent voltage (which could be taken from the available PTAT or CTAT components) applied to the gate terminal is expressed as

\[
V_{GS}(T) = V_{GS0} + \gamma(T - T_0),
\]

where \( V_{GS0} \) is the gate-source voltage at the nominal value and \( \gamma \) is a positive (for PTAT case) or negative (for CTAT case) constant.

1) **Saturation Region:** Replacing (3), (4) and (6) into (1) for the saturation case, \( I_D \) can be written as

\[
I_D(T) = K_1(\frac{T}{T_0})^{-m}[V_0 + \lambda(T - T_0)]^2,
\]

where \( K_1 = \frac{1}{2} W L \mu_0 C_{ox}, V_0 = V_{GS0} - V_{TH0}, \) and \( \lambda = (\gamma + aVT) \). Following the approach in [13], [14], if the temperature raises by a small amount \( \delta T \) from \( T_0 \) to \( (T_0 + \delta T) \), then:

\[
I_D(T_0 + \delta T) = K_1(1 + \frac{\delta T}{T_0})^{-m}[V_0 + \lambda \delta T]^2.
\]

Using the Taylor series expansion

\[
(1 + \frac{\delta T}{T_0})^{-m} \approx (1 - m \frac{\delta T}{T_0}),
\]

and subtracting \( I_D(T_0) = K_1 V_0^2 \) from (8), the change in \( I_D \) with temperature is estimated to be

\[
\delta I_D = \delta T [K_1 V_0(2\lambda - \frac{mV_0}{T_0})] + \delta T^2 [K_1 \lambda(\lambda - \frac{2mV_0}{T_0})] - \delta T^3 [K_1 \frac{m^2 \lambda^2}{T_0^2}].
\]

2) **Deep triode Region:** Same discussion can be applied for the drain current in the deep triode region. Using (3), (4), (6) and (9), and ignoring the temperature dependency of \( V_{DS} \), the change in \( I_D \) from (1) for the deep triode region when the temperature changes from \( T_0 \) to \( T_0 + \delta T \) can be estimated as

\[
\delta I_D = \delta T^2[2K_1 \lambda - \frac{2K_1 m V_0}{T_0}] - \delta T^3[2mK_1 \lambda^2].
\]

3) **Subthreshold Region:** In the subthreshold region, the drain current follows (5), where \( V_T = kT/q \), with \( k \) being the Boltzmann constant and \( q \) the electron charge. The term inside the exponential function in (5) can be written as:

\[
\frac{(V_{GS} - V_{TH})}{nkT/q} = \frac{\lambda}{nk/q} + \frac{1}{T} \left[ \frac{\lambda T_0}{nk/q} - \frac{\lambda T}{nk/q} \right] = A_0 + A_1 T^{-1},
\]

where \( A_0 = \frac{\lambda}{nk/q} \) and \( A_1 = \frac{\lambda T_0}{nk/q} - \frac{\lambda T}{nk/q} \). \( A_1 \) is generally a negative term. Noting \( K' = 2K_1(n-1)(\frac{T_0}{q})^2 \), the current \( I_D \) from (5) can be rewritten as

\[
I_D(T) = K'(\frac{T}{T_0})^{-(2-m)} \exp(A_0 + A_1 T^{-1}).
\]

Using the Taylor expansion of \( \frac{1}{1 + \frac{\delta T}{T_0}} \approx 1 - \frac{\delta T}{T_0} \), the change in the drain current when the temperature varies from \( T_0 \) to \( (T_0 + \delta T) \) is estimated to be

\[
\delta I_D = I_D(T_0)\left[(1 + (2 - m) \frac{\delta T}{T_0}) \exp(\frac{-A_1 \delta T}{T_0}) - 1 \right].
\]
Fig. 2. Realization of case 1-a using NMOS transistors.

Equations (10), (11), and (14) clearly show that $I_D$ in each operating region has non-linear behavior with temperature and depending on the value of $\gamma$ and $V_0$, the weighted contribution of each term could be different.

B. Multi-Piecewise Curvature-Corrected Technique

We now discuss the four possible conditions shown in Fig. 1, and see how by controlling the temperature behavior of the gate-source voltage (through $\gamma$) one can generate different non-linear components.

1) Case I-a: As seen in Fig. 1, case 1-a refers to the condition in which as the temperature passes $T_{\text{CRITICAL}}$, the transistor switches from operating in the subthreshold to either the deep triode or saturation region. For this case, the gate voltage has to be an increasing function of temperature, and hence, one option is to use the already available PTAT current from the uncompensated BGR. Fig. 2 shows one circuit realization option for this approach, where the gate-source voltage of the transistor $M_1$ is set by the voltage across resistor $R$ through which a mirrored version of the available PTAT current is flowing. Fig. 2-b corresponds to the case of $M_1$ switching into the deep triode region, since a diode-connected transistor $M_2$ is included in the circuit to decrease the $V_{DS}$ of $M_1$. As seen from (11), when a PTAT voltage is applied to the gate terminal ($\gamma > 0$), the drain current will be increasing with temperature and with the first order term being the dominant term. Fig. 2-c shows the case when $M_1$ will be switching into the saturation region.

2) Case I-b: In case 1-b, the gate-source voltage is a decreasing function of temperature, therefore, the behavior of the drain current over the temperature will be the mirrored version of the currents in case 1-a, around a reference plane set at $T_{\text{CRITICAL}}$. Currents from case 1-b can be used to fulfill the demand of compensation in the low temperature region. The design in [5], being implemented with PMOS transistors, is similar to case 1-b. Fig. 3 shows the results of corner simulations for the current $I_D$ of an NMOS transistor biased to meet the conditions of cases 1-a and 1-b. For each case, transition to and from the deep triode region (Figs. 3(a) and 3(b)) and saturation region (Figs. 3(c) and 3(d)) are considered. As can be seen, the temperature behavior of the currents follow the pattern predicted in Section II.

3) Cases I-c and I-d: In these two cases, the transistor remains in the subthreshold region. Equation (14) shows that

C. PMOS vs NMOS implementation

Both NMOS and PMOS transistors can be used for the realization of the four cases shown in Fig. 1. Implementation using NMOS transistors results in generating current sources (which can be used for adding the nonlinear terms to existing currents, as is the case in most of the existing piecewise compensation techniques), while with PMOS transistors, current sinks are implemented, which can be employed as current subtractor. Fig. 5 illustrates how using a current sink can become effective
in reducing the temperature coefficient of a BGR circuit.

IV. DESIGN CONSIDERATION

Depending on the behavior of the BGR’s output across the desired temperature range, our proposed solution can be used to minimize its temperature coefficient. Proper design considerations need to be followed to maximize the compensation. First is the selection of $T_{\text{CRITICAL}}$ point. As seen in Fig. 2, resistor $R$ can be used to control the value of $V_{\text{GS}}$, and therefore, the value of $T_{\text{CRITICAL}}$. A good practice would be to use a tunable resistor [15] and be able to move the location of $T_{\text{CRITICAL}}$, if needed.

Looking at the current outcomes of the four cases presented in Fig. 1, a proper combination of these conditions can be used to achieve the maximum compensation. In addition, an array of different piecewise blocks can be designed as a trimming network, to tune the temperature coefficient of the circuit after fabrication.

V. A DESIGN EXAMPLE

To validate the effectiveness of this technique, a first-order BGR circuit was designed in IBM 8HP process. The schematic is shown in Fig. 6. The PTAT current is generated by the difference between base-emitter voltages of two transistors with different emitter areas. A voltage-mode compensation is achieved by adding the base-emitter voltage of transistor $Q_2$ and the PTAT voltage across $R_1$ [1]. The circuit shows a temperature coefficient of 13.7 ppm/°C over (-50:100)°C temperature range (Fig. 7). To improve the temperature stability of the circuit, two piecewise compensation blocks were designed. One block is implemented using NMOS transistors for the condition of switching from subthreshold to saturation region (case 1-a), while another one is realized by PMOS transistors to cover the reverse switching condition (Fig. 7). The critical temperature of each block was determined separately. With the aid of these two compensation blocks, the temperature coefficient of the circuit is significantly decreased to 0.6 ppm/°C (Fig. 7), which demonstrates the effectiveness of the proposed technique.

VI. CONCLUSION

A multi-piecewise curvature-corrected compensation technique based on controlling the temperature behavior of the gate-source voltage of MOSFETs is proposed. Four different cases for generating piecewise currents are considered and a detailed analysis of the expected temperature behavior is provided. The technique provides the designer with additional flexibility to achieve the maximum temperature compensation. To examine the effectiveness of the proposed technique, a first-order BGR circuit with a temperature coefficient of 13.7 ppm/°C was designed. Simulation results showed that the proposed multi-piecewise curvature-corrected technique improved its temperature coefficient to 0.6 ppm/°C.

REFERENCES