Towards Temperature-Stable Level Shifters

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***Abstract*—A family of temperature stable level shifter circuits, covering a wide range of voltage level shifts, is presented in this paper. Design analysis is provided for both shift-up and shift-down circuits. Circuits are designed in 0.13 μm BiCMOS technology, and simulation results are presented.**

Keywords-BiCMOS, Lever Shifters, Temperature Stability.

I. Introduction

Energy efficiency is one of today's key design challenges for electronics used in portable systems. Several approaches have been proposed to reduce the static/dynamic power consumption, including voltage scaling, optimum sizing, and switching activity reduction, with voltage scaling being the most efficient technique [1]-[3]. For system-on-chip designs, where requirements of voltage scaling vary for different circuit blocks, multi-supply voltage technique is being used [4]. In such cases, level shifters are necessary part of the design to provide necessary voltage level conversion. Level shifters are also being used in various analog and mixed-signal circuits, including operational amplifiers and comparators [5].

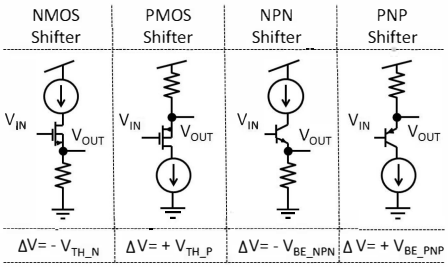

Fig. 1. Conventional simple level shifter circuits.

At its simplest level, a CMOS/BJT transistor can be used to shift the DC level of the input voltage, up or down, by the threshold voltage (V_{TH})/base-emitter voltage (V_{BE}) value of the shifting transistor (Fig. 1). Both V_{TH} and V_{BE} vary with temperature [6], [7] and therefore, the generated DC level shift from these circuits will become temperature dependent. This temperature dependency of the DC level is generally undesired, specially for applications requiring highly stable conversion level. To address this issue, a simple technique for the realization of temperature-stable level shifters is presented. This paper is organized as follows. In Section II the basic concepts are given. The proposed design technique is described in Section III. Design considerations are presented in Section IV, and conclusions are given in Section V.

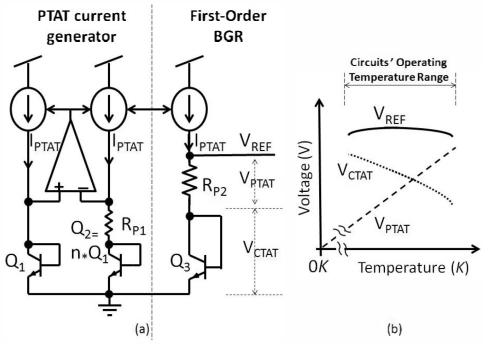

Fig. 2. Conventional first order voltage mode bandgap references.

II. Basic Concepts

For an NMOS transistor, V_{TH} decreases approximately linearly with temperature as [8]

$$V_{TH} = V_{TH0} - \alpha_{VT}(T - T_0), \tag{1}$$

where α_{VT} is a positive number, and V_{TH0} is the threshold voltage at the reference temperature T_0. In the case of BJTs, V_{BE} is also a decreasing function of temperature which can be expressed as [7]

$$V_{BE} = \beta_1 + \beta_2 T + \beta_3[T\ln(T)] + \beta_4[T\ln(I_C)], \tag{2}$$

where

$$\beta_1 = V_{g0}, \quad \beta_2 = \frac{k}{q}\ln(\frac{T_0^m}{I_{C0}}) - \frac{(V_{g0} - V_{BE0})}{T_0}$$

$$\beta_3 = -\frac{mk}{q}, \quad \beta_4 = \frac{k}{q},$$

and V_{g0} is the extrapolated bandgap voltage of Si at 0 K, T is the absolute temperature in K, I_{C0} and V_{BE0} are the collector current and base-emitter voltage at T_0, respectively, and m is a positive constant.

Bandgap Reference circuits (BGRs) are designed to generate temperature independent voltages/currents. Typically, in BGRs, temperature compensation to the first degree is achieved by proper addition of a complementary-to-absolute-temperature (CTAT) voltage/current and a proportional-to-absolute-temperature (PTAT) voltage/current [7]. Fig. 2 shows the schematic of a typical BGR circuit, and its simulated output voltage over temperature range of -55 °C to 125 °C.

From Fig. 2-a, the PTAT current can be expressed as [7]

$$I_{PTAT} = \frac{V_{BE,1} - V_{BE,2}}{R_{P1}} = V_T\frac{\ln(n)}{R_{P1}} = \beta_5 T, \tag{4}$$

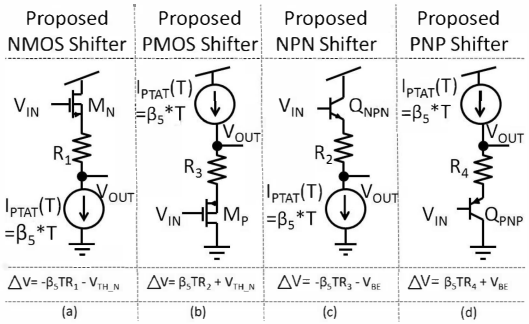

Fig. 3. Proposed temperature stable level shifter circuits..

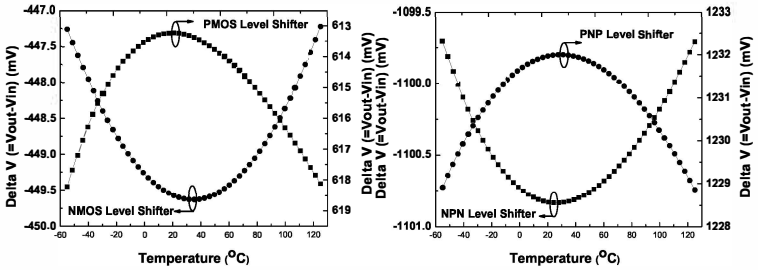

Fig. 4. ΔV over temperature of (a)MOS-based (b)BJT-based level-shifter circuits.

where $V_T = \frac{kT}{q}$ is the thermal voltage, n is the emitter area ratio of Q_2 over Q_1, and $\beta_5 = \frac{k \times \ln(n)}{q \times R_{P1}}$. This PTAT current is being mirrored and flown through resistor R_{P2}, generating a PTAT voltage. Proper addition of this voltage with V_{BE} of transistor Q_3 will produce a first-order temperature-compensated voltage at the V_{REF} node.

III. Proposed Design Technique

Motivated by the idea behind the temperature compensation in BGR circuits, a family of temperature-stable DC level shifter circuits is proposed and illustrated in Fig. 3. In all four designs, the shifting-level transistors are biased by PTAT currents. Both level-down (Figs. 3-a, 3-c) and level-up (Figs. 3-b, 3-d) shifters have been considered. In what follows, without loss of generality, the operation of NMOS-based level-down and PNP-based level-up shifters have been described. However, the concepts can be easily extended to PMOS-based level-up and NPN-based level-down shifters.

A. Temperature-Compensated Level-Down Shifter

Fig. 3-a represents an NMOS-based level-down shifter. Transistor M_N is biased by the PTAT current $\beta_5 T$. In conventional level-shifters, the output is taken from the source terminal of the shifting transistor (Fig. 1). Here, a resistor R_1 is introduced between the source terminal and the output node. Using (1) and (4), the DC shift level, ΔV, can be derived as

$$\begin{aligned} \Delta V(T) &= V_{OUT} - V_{IN} = [-V_{TH,N}(T)] - [\beta_5 T \times R_1] \\ &= -V_{TH0} + \alpha_{VT}(T_0) + (\alpha_{VT} - \beta_5 T R_1)T. \end{aligned} \quad (5)$$

Equation (5) indicates that when $\alpha_{VT} = \beta_5 T R_1$, a temperature insensitive level-down shifting can be obtained.

B. Temperature-Compensated Level-Up Shifters

A temperature compensated level-up shifter involving a PNP transistor is shown in Fig. 3-d. Transistor Q_{PNP} is driven by the PTAT current $\beta_5 T$. Ignoring the high-order temperature dependent terms in (2), the V_{EB} of Q_{PNP} can be expressed as

$$V_{EB} \approx \beta_1 + (\beta_2 + \beta_4 \ln \beta_5)T. \quad (6)$$

The DC shift level, ΔV, can then be obtained as

$$\begin{aligned} \Delta V(T) &= [V_{EB}(T)] + [\beta_5 T \times R_4] \\ &\approx \beta_1 + (\beta_2 + \beta_4 \ln \beta_5 + \beta_5 R_4)T. \end{aligned} \quad (7)$$

The temperature compensation problem turns into the same scenario as the first order BGR circuit shown in Fig. 2.

IV. Simulation Results and Discussions

Temperature-compensated level shifter circuits for all four cases shown in Fig. 3 were designed in IBM's $0.13\mu m$ BiCMOS technology, and simulated across the temperature range of (-55:125)°C. The circuits operated with a power supply of 2.5 V. Fig. 4 shows simulation results for ΔV ($\Delta V = V_{OUT} - V_{IN}$) as a function of temperature for four cases, illustrating that temperature-stable level shifts, at different levels (mV and V, shift-down and shift-up), have been obtained from all cases. The four designs presented here offer a family of DC analog level shifters that can cover a wider range of voltage-shifts for designers.

V. Conclusion

In this paper, a family of simple temperature-stable level shifter circuits were introduced. Circuits were designed in IBM's 0.13 μm technology, and were simulated across temperature validating their stability.

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