Potential Questions for Exam I — 332:416 Control Systems Design

EXAM I: Thursday, March 11, **2004**, 9:50–11:10

Closed Book and Notes. No Calculators.

1) Define the gain and phase stability margins and the gain and phase crossover frequencies by using the Nyquist plot. (GL96, pages 206–207).

2) Define the system transient response parameters and explain the procedure for finding these parameters. (GL96, Sections 6.1 and 6.2, pages 262–269).

3) Explain the importance of system dominant poles for finding the transient response parameters of high-order systems. (GL96, Section 6.3, pages 269–272).

4) Define and derive steady state response errors for linear feedback control systems (GL96, Section 6.4, pages 276–281).

5) Explain the essence of the root locus technique. (GL96, Section 7.1, pages 291–296).

6) Define the minimum phase linear systems and explain why the nonminimum phase systems should be treated with a special care (GL96, page 317).

7) Explain the effect of a stable dipole on the root locus and the system transient response (GL96, Section 8.5.1, pages 343–345).

8) Present design algorithms for PI and phase-lag controllers based on the root locus technique and comment on their main features (GL96, Section 8.5.1, pages 345–352).

9) Present design algorithms for PD and plase-lead controllers based on the root locus technique and comment on their main features (GL96, Section 8.5.2, pages 353–363).

10) Present design algorithms based on the root locus technique for PID and phase-lead-lag controllers and comment on their main features (GL96, Section 8.5.3, pages 364–369).

11) Show how to read from Bode diagrams the phase and gain margins, phase and gain crossover frequencies, and steady state constants (GL96, Sections 9.3.1–9.3.2, pages 392–398).

12) Plot the Bode diagrams for the phase lead controller and find its maximal phase and the frequency at which the phase maximum occurs (GL96, Section 9.4.2, pages 402–403).

13) State four main principles used in Bode diagram control design techniques (GL, Section, 9.4, p. 399).

14) Describe the phase-lead controller design algorithm based on Bode diagrams (GL96, Section 9.4.4, page 405, Algorithm 9.1).

15) Describe the phase-lag controller design algorithm based on Bode diagrams (GL96, Section 9.4.5, pages 410–411, Algorithm 9.2).

16) Derive the observability rank conditions for both discrete- and continuous-time linear systems (GL96, Sections 5.1–5.2, pages 223–226).

17) Derive the controllability rank condition for discrete-time, single-input single-output, linear systems (GL96, Section 5.3, pages 227–228).

18) State the frequency domain controllability and observability test (GL96, Section 5.5, page 235).

19) Explain the full-order observer design technique and draw the corresponding block diagram. Give the observer equations, the equation for the observation error, and explain a rational choice for observer poles. (GL96, Sections 5.6–5.6.1, pages 241–243).

20) Explain and justify the separation principle in the context of the observer design problem. (GL96, Section 5.6.1, pages 243–244).

21)* Present the essence of the reduced-order observer design (GL96, Section 5.6.2, pages 244–247).

22) Describe the pole placement design technique for linear control systems represented in phase variable canonical form (GL96, Section 8.2, pages 333–335).

* QUESTION 21 WILL NOT BE ON EXAM 1.