A Comprehensive Understanding of the Efficacy of N-Ring SEE Hardening Methodologies in SiGe HBTs

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***Abstract*—We investigate the efficacy of mitigating radiation-based single event effects (SEE) within circuits incorporating SiGe heterojunction bipolar transistors (HBTs) built with an N-Ring, a transistor-level layout-based radiation hardened by design (RHBD) technique. Previous work of single-device ion-beam induced charge collection (IBICC) studies has demonstrated significant reductions in peak collector charge collection and sensitive area for charge collection; however, few circuit studies using this technique have been performed. Transient studies performed with Sandia National Laboratory's (SNL) 36 MeV ^{16}O microbeam on voltage references built with N-Ring SiGe HBTs have shown mixed results, with reductions in the number of large voltage disruptions in addition to new sensitive areas of low-level output voltage disturbances. Similar discrepancies between device-level IBICC results and circuit measurements are found for the case of digital shift registers implemented with N-Ring SiGe HBTs irradiated in a broadbeam environment at Texas A&M's Cyclotron Institute. The error cross-section curve of the N-Ring based register is found to be larger at larger ion LETs than the standard SiGe register, which is clearly counter-intuitive. We have worked to resolve the discrepancy between the measured circuit results and the device-level IBICC measurements, by re-measuring single-device N-Ring SiGe HBTs using a time-resolved ion beam induced charge (TRIBIC) set-up that allows direct capture of nodal transients. Coupling these measurements with full 3-D TCAD simulations provides complete insight into the origin of transient currents in an N-Ring SiGe HBT. The detailed structure of these transients and their bias dependencies are discussed, together with the ramifications for the design of space-borne analog and digital circuits using SiGe HBTs.**

***Index Terms*—HBT, N-ring hardening, RHBD, SEE, SEU, SiGe, silicon-germanium technology.**

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I. Introduction

A. Motivation

SYSTEM-ON-CHIP (SoC) solutions have the capability of minimizing total costs and reducing pay-load sizes for orbital missions—qualities that are extremely desirable for space applications. Silicon-germanium (SiGe) BiCMOS platforms have quickly become recognized as strong contenders for SoC space applications given the excellent low-temperature performance of the SiGe HBT and its built-in multi-Mrad total ionizing does immunity (TID); however, this technology suffers from aggravated sensitivities to single event effects (SEEs) that can range from benign data loss to complete system failures [1]. Substantial research has led to a wide variety of topological circuit modifications [2], [3] and device layout schemes [4], [5] which aim to minimize the sensitivity of SiGe HBTs to SEEs. The most successful of these RHBD procedures (triple modular redundancy and gated-feedback cells) are circuit-level architectures which require substantial penalties in area and power consumption, leading to an overall increase in pay-load cost. Given these drawbacks, it is more desirable to investigate hardening methodologies which employ device-level modifications that do not require additional mask layers (i.e., maintains standard fabrication costs).

One such technique that has received significant attention is the incorporation of a "dummy collector" or "N-Ring" n+ implant around the perimeter of the trench isolation of an NPN SiGe HBT [6], [7]. A cross-section comparison of a standard SiGe HBT and an N-Ring SiGe HBT is presented in Fig. 1. The additional reversed-biased junction formed by the N-Ring-substrate serves to shunt generated carriers, from ion strikes through the substrate, away from the sensitive subcollector-substrate junction. This technique is theorized to be most effective for ion-strikes occurring outside the trench isolation of the HBT, reducing the total sensitive area to transient effects while having a minimal impact on the transient profiles of ion-strikes within the active area (especially emitter-center) of the HBT.

To date, primarily only single transistor studies have been performed on this radiation hardening by design (RHBD) technique, using ion beam induced charge collection (IBICC) measurements by means of a heavy-ion microbeam [7]. These experiments show promising results for reducing peak collector charge collection as well as shrinking the sensitive area of the device. Motivated by these results, N-Ring SiGe HBTs were integrated into both an analog (a SiGe bandgap reference) and a digital (a 16-bit standard master/slave serial shift register) circuit and tested in-beam. These circuits were designed and developed using IBM's 1st generation (f_T of 46 GHz and f_{max}

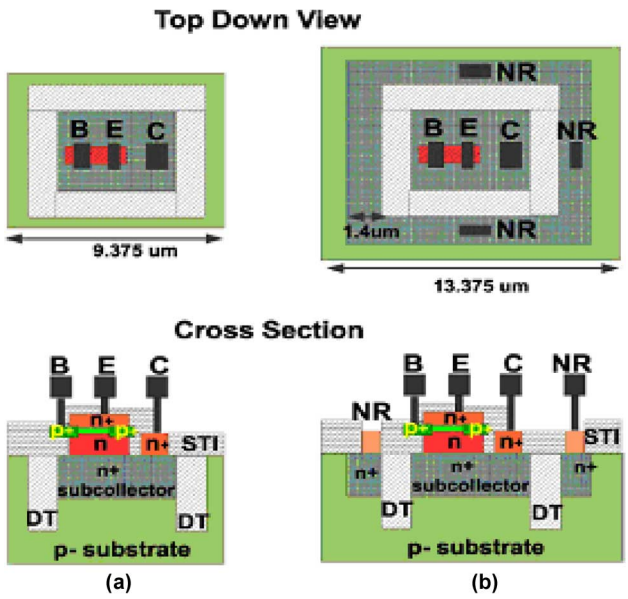

Fig. 1. Top down and cross-sectional views of the (a) standard SiGe HBT and the (b) N-Ring variant from [8].

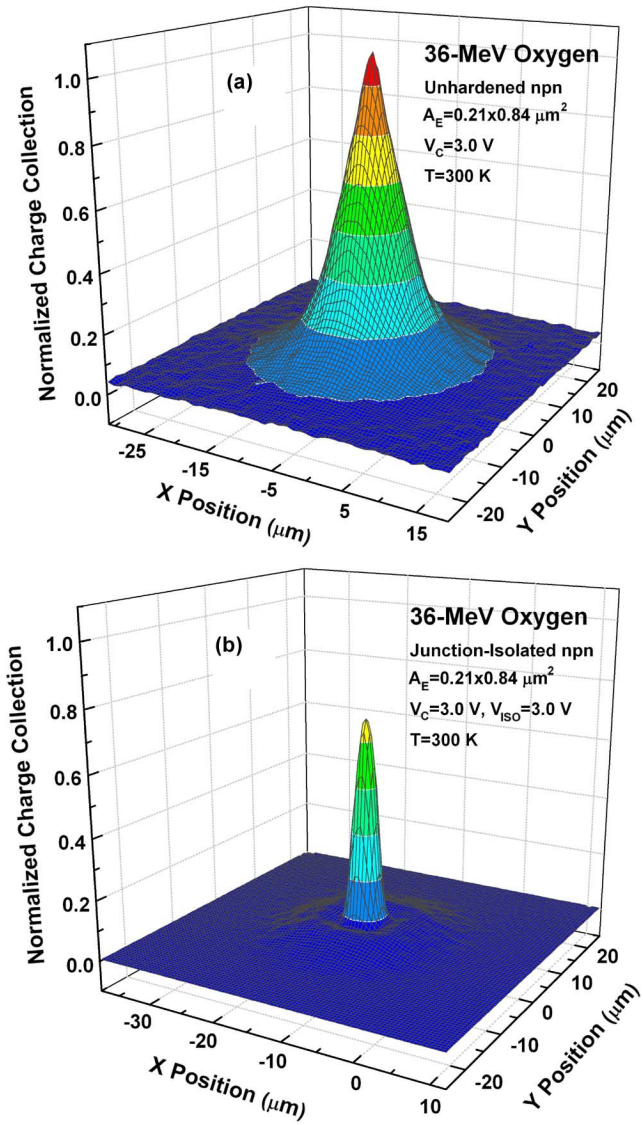

Fig. 2. Normalized (to peak charge of standard device) charge collection measurements of the (a) standard SiGe HBT and the (b) N-Ring SiGe HBT performed using SNL's 36 MeV ^{16}O microbeam from [10].

of 65 GHz) SiGe BiCMOS platform. The analog circuit results have been reported previously [8], whereas the digital circuit results are shown here for the first time. We find strikingly different circuit results when compared to the expected response predicted by the single device IBICC measurements. In the present paper we have worked to eliminate the discrepancy between the measured circuit results and the device-level IBICC measurements by re-measuring single device N-Ring SiGe HBTs using a time-resolved ion beam induced charge collection (TRIBICC) set-up that allows direct capture of nodal transient currents. Coupling these measurements with full 3-D TCAD simulations provides complete insight into the origin of transient currents in an N-Ring SiGe HBT. The detailed structure of these transients and their bias dependencies are discussed, with implications for both analog and digital circuits.

B. Review of N-Ring IBICC Results

Ion beam induced charge collection measurements rely on charge-sensitive preamplifiers to integrate unipolar transient signals on device terminals to provide a measure of total nodal-induced charge. This technique has classically been used to test solid-state memory cells (e.g., SRAM), where a known metric of "critical charge" for digital upset is used as a foundation to ascertain cell sensitivity [9]. Although less applicable to SiGe HBT digital logic, where non-zero steady-state current flows regardless of the digital state, the IBICC technique is desirable given its insensitivity to time distortions of the transient waveform. Given that the total amount of charge induced on a device terminal is conserved regardless of any filtering of the waveform, very simple packaging of the device under test can be performed, disregarding any parasitic capacitances or inductances that may be present. Standard and N-Ring SiGe HBTs have been tested using the IBICC measurement set-up at Sandia National Laboratory's heavy-ion microprobe facility on various SiGe industry platforms and generations, as reported in the IBICC studies reported previously in [6], [7], [10]. With typical results reprinted in Fig. 2, the trend in nearly eliminating collector-induced charges for ion-strikes external to the trench isolation of the HBT is seen across several industry platforms. A second fact from this figure to be discerned is that the collector-induced charge for ion-strikes through the center of the active area of the device is reduced for this technology with shallower trench isolation [10] when N-Rings are employed. Previous studies in technologies with deeper trench isolation [6] have not shown the same magnitude of reduced collector charge for ion strikes through the center of the active area. The origin for this improved mitigation can be attributed to the increase in ambipolar diffusion as a result of less trench trapping of charges, as discussed in [11], which allows ionized charge to be swept into the N-Ring-substrate junction. Given the significant reduction in measured sensitive area and total peak collector charge collection of the N-Ring HBTs reported for the IBICC results, it would be expected that the digital

systems built from these structures would show improved error performance in a heavy-ion broadbeam environment.

II. Experiment Details

Despite these promising IBICC results, in order to truly evaluate the efficacy of mitigating single event effects through the incorporation of an N-Ring SiGe HBT, it is necessary to test circuits which contain these structures. While considerable work has been performed in characterizing digital components to single event phenomena, a distinct trend of rising interest are the effects of transient phenomena on analog and mixed-signal circuits [12], [13]. Consequently, we have constructed digital shift registers and precision analog voltage references using both standard and N-Ring SiGe HBTs to facilitate beam testing to probe single event sensitivities. Single SiGe HBTs encompassing N-Rings were also packaged for time-resolved ion beam induced charge (TRIBIC) measurements; a method which directly captures the induced current transient waveforms on device terminals due to an ion strike event, providing information on the transient's amplitude, polarity, and duration. Two facilities were used to provide the beam environments needed to test the analog, digital, and single-device structures: Sandia National Laboratory's Nuclear Microprobe Facility [14] and Texas A&M's Cyclotron Institute [15].

A. Heavy-Ion Microprobing

Both the voltage references and the stand alone SiGe HBTs were irradiated using SNL's heavy-ion microbeam. The packaging and experimental conditions of the SiGe voltage references have been covered previously in [8]. The data collected from SNL's microbeam provided relative spatial coordinates for each normally incident 36 MeV ^{16}O ion strike giving an estimated peak LET of 7 $(\mathrm{MeV} * \mathrm{cm}^2/\mathrm{mg})$ as determined from SRIM calculations [16]. The stand-alone HBTs (standard and N-Ring structures) had an emitter area of $0.5 \times 2.5\ \mu\mathrm{m}^2$. Semiconductor wafers were packaged die-on-board using a custom high-speed, hybrid printed circuit board that facilitated high-bandwidth 50 Ω transmission lines and maintained board rigidity. A thin Rogers 4003 C dielectric was selected to provide the desired 50 Ω microstrip widths as well as a suitable low value of loss tangent. Device terminals were wire-bonded to the microstrip lines using 1.0 mil gold wire that terminated to through-hole 18-GHz subminiature version A (SMA) connectors. The experimental set-up is nearly identical to previous TRIBIC experiments where the parasitic components have been analyzed in detail [17]. The devices under test (DUTs) were irradiated with a 1.0 V bias on the collector and the base and all other terminals grounded; the N-Ring devices had the additional N-Ring terminal that was held at 3.3 V. These bias conditions were similar to the bias conditions of the sensitive structure in the voltage regulator circuit. The oxygen ion beam was rastered across each device, providing a spatial map of transient waveforms for given coordinates. Transients were captured from all terminals of the standard SiGe device (collector, base, emitter, and substrate) and the collector, base, N-Ring, and substrate terminals for the N-Ring SiGe device, using a Tektronix DPO72004 real-time oscilloscope.

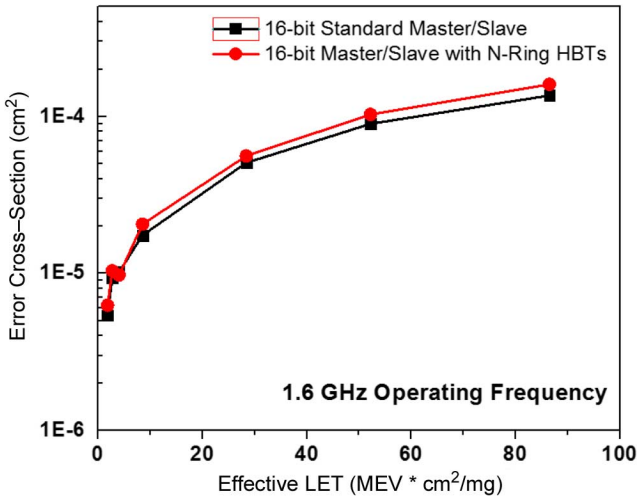

Fig. 3. Error cross-section curve for a standard and N-Ring variant 16-bit SiGe shift register operating at 1.6 Gbps.

B. Heavy-Ion Broadbeam Testing

The digital circuits tested included two 16-bit master/slave serial shift registers—one composed of standard SiGe HBTs, while the second was built with N-Ring SiGe HBTs. The registers were completely identical in their architecture, clock distribution, operation frequency, and power dissipation. These circuits were irradiated at Texas A&M's Cyclotron Institute's heavy-ion broadbeam facility and tested in-beam with an Agilent MP1764 BERT analyzer utilizing a 127-bit pseudo-random input data sequence. The registers were operated with a 5.2 V rail (the N-Rings were held at this potential) and at a frequency of 1.6 Gbps. Bit upsets were recorded during exposure as well as the total fluence, permitting the construction of a full error cross-section curve. The TAMU facility provided a wide range of very high-energy ions with various LETs that have no recorded spatial correlation with strike events. Heavy ion exposures included 15 MeV/amu ^{197}Au, ^{129}Xe, ^{84}Kr, ^{40}Ar, ^{20}Ne and 25 MeV/amu ^{22}Ne giving LETs of 86.5, 52.2, 28.4, 8.5, 2.7, and 1.8 MeV $\mathrm{cm}^2/\mathrm{mg}$ respectively. All DUTs were exposed at normal incidence.

III. Measured Results

The measured error cross-section curves generated for both standard and N-Ring shift registers are plotted in Fig. 3. The error bars associated with the measurements overlap with the data point when plotted on a log-linear scale. While the threshold linear energy transfer (LET) for both registers is identical, the saturated error cross-section is distinctly larger for the N-Ring SiGe shift register. This result is counter intuitive in light of the results from the single-device IBICC studies performed on N-Ring SiGe HBTs. Given the significant measured reduction in sensitive area and total peak collected charge of the N-Ring HBTs reported for the IBICC results, it would be expected that the N-Ring shift register would show improved error performance. We also had previously observed this discrepancy between IBICC measurements and circuit results in the analog voltage regulators [8]. The voltage references built

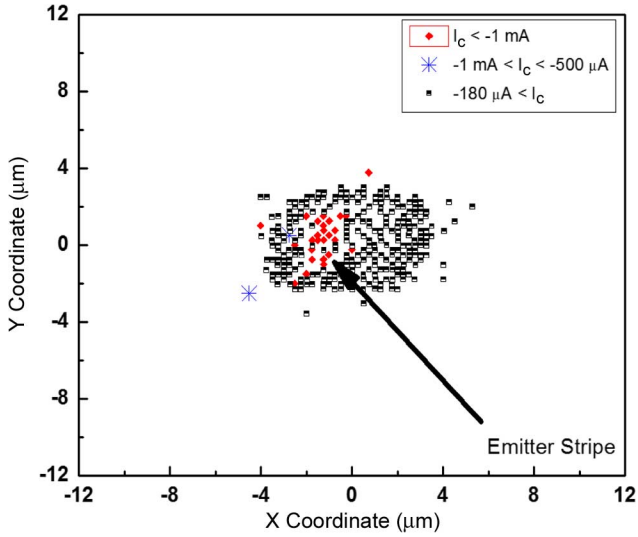

Fig. 4. Peak transient collector current amplitude plotted against the X-Y coordinates of the ion strike position for a standard SiGe HBT.

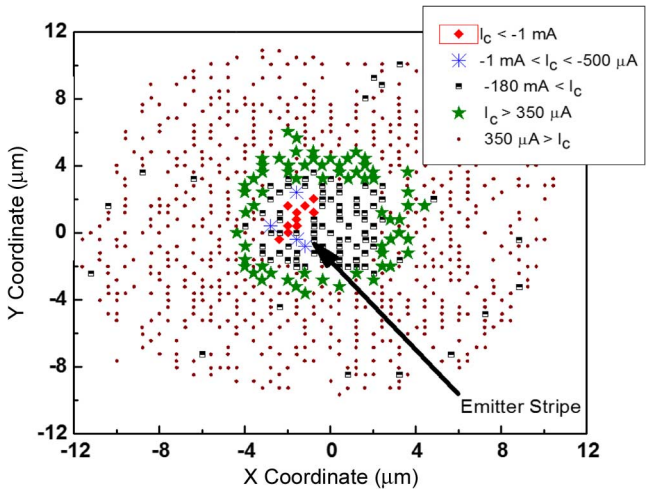

Fig. 5. Peak transient collector current amplitude plotted against the X-Y coordinates of the ion strike position for an N-Ring SiGe HBT

with SiGe N-Ring SiGe HBTs showed additional sensitive regions to transient phenomena that weren't present in the voltage references constructed with standard SiGe HBTs. However, the N-Ring voltage reference also showed a reduction in the number of transient events with large amplitudes. To interpret the complex set of results captured from the analog and digital circuit exposures and explain the discrepancy between the single-device IBICC measurements, TRIBIC experiments were performed on single SiGe HBTs with and without N-Rings.

An easy visualization of the results of a TRIBIC measurement can be created by mapping the peak transient amplitude of a specified terminal as a function of the recorded position of the transient event. Given that the primary sensitive terminal for the circuits we have tested is the collector, this terminal was selected for imaging the transient response. This terminal selection is not applicable to all circuit types, however, as has been shown in previous investigations of emitter-followers [18]. The transient map for the standard device is shown in Fig. 4, whereas the transient map for the N-Ring device is shown in Fig. 5. A comparison of the two maps clearly shows that the N-Ring HBT has a much larger sensitive area for transients on the collector terminal. These results are a striking contradiction to earlier IBICC measurements that have shown reductions in the sensitive area of an N-Ring HBT [6], [10]. Despite the difference in total sensitive area, both devices show the same characteristics for transients induced by ion strikes internal to the deep trench; namely, the peak transient collector current is negative in polarity, indicating current flowing into the collector terminal. The most sensitive region for maximum transient signatures within the deep trench is through the emitter of the device, where a normally incident ion will pass through all the sensitive junctions. Fig. 6 presents a comparison between the collector transient signals for each device type due to emitter-center strikes. These transients are similar, with slight reductions in peak amplitude for the N-Ring device. The magnitude of this reduction will vary depending on the depth of the deep trench isolation layer, with shallower trenches resulting in greater attenuation.

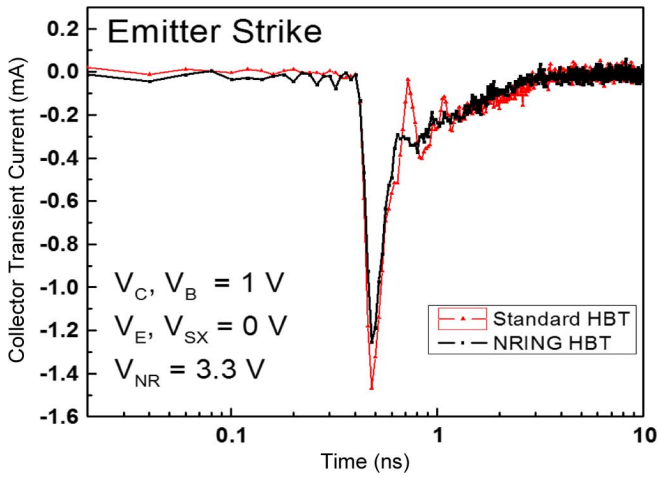

Fig. 6. Measured transient waveforms on the collector terminal induced by an emitter ion strike for both a standard and N-Ring SiGe HBT.

The difference in sensitive area between the two device types arises from the presence of collector transients external to the trench isolation for the N-Ring HBT. These signals have maximum peak transient amplitudes that are positive in polarity—opposite to that of strikes occurring internal to the trench isolation. The area of maximum sensitivity for these positive polarity transients occurs for ion strikes directly through the N-Ring-substrate depletion region. It can be thus be inferred that there is a coupling phenomena occurring between the device collector and the N-Ring terminal. In Fig. 7, typical transient waveforms arising from a normally incident oxygen ion strike to the N-Ring region for the collector, base, N-Ring, and substrate terminals are plotted. As reflected in the transient map, the collector transient has a peak amplitude that is positive; in addition, the collector signal has a bipolar signature. This bipolar nature of the collector transient waveform accounts for the discrepancy between the TRIBICC and IBICC results. The IBICC set-up requires charge-sensitive preamplifiers which integrate the transient waveforms to give a measure of the total charge induced on a device terminal and are limited

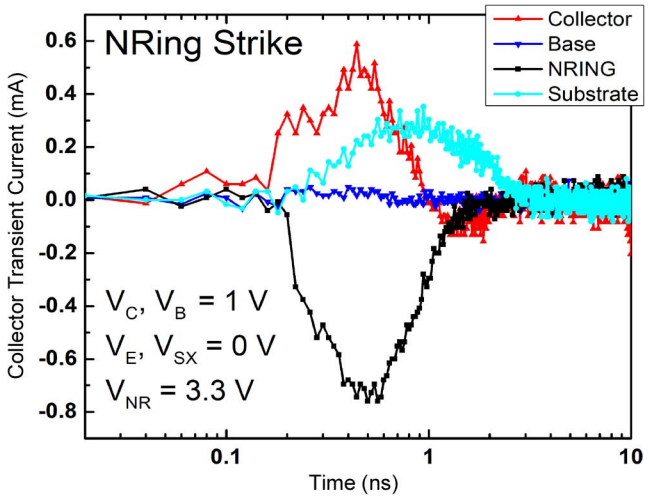

Fig. 7. Measured transient waveforms induced on the collector, base, N-Ring, and substrate due to an N-Ring ion strike of an N-Ring SiGe HBT. The collector transient displays a bipolar signature.

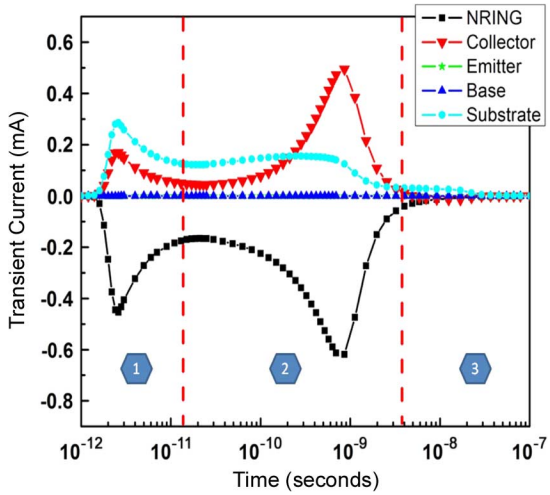

Fig. 9. Simulated transient waveforms for an ion strike through the N-Ring of an N-Ring SiGe HBT biased with 3.3 V on the N-Ring and with all other terminals ground.

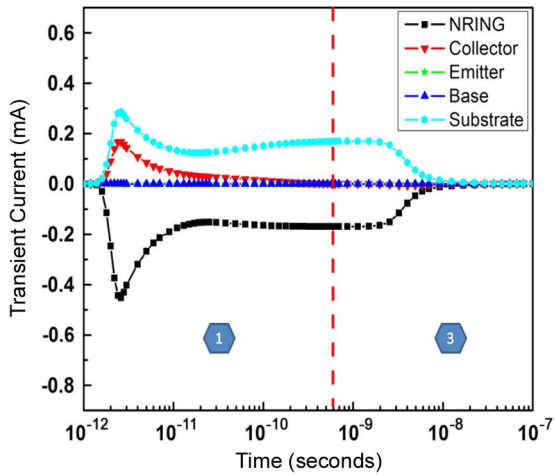

Fig. 8. Simulated transient waveforms for an ion strike through the N-Ring of an N-Ring SiGe HBT biased with 3.3 V on the N-Ring and collector and with all other terminals ground.

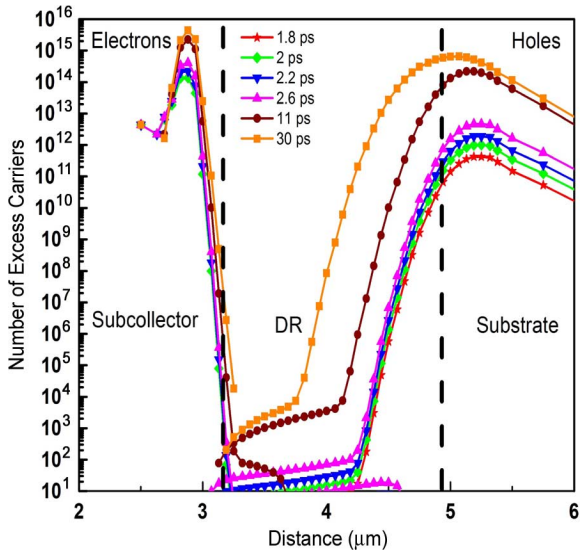

Fig. 10. Excess electron and hole concentrations following an ion strike on either side of the depletion region (DR) of the subcollector-substrate junction.

to only unipolar signals. Bipolar signals will potentially lead to cancellation of integrated charges, giving erroneous values of total induced charge. With this in mind, we use calibrated 3-D TCAD simulations to fully understand the origin of these positive collector transients and their bipolar nature.

IV. 3D TCAD Simulations

The 3D device decks were calibrated to the DC characteristics for both the standard and N-Ring first generation SiGe device using CFDRC's NanoTCAD software package [19]. A top side substrate contact was incorporated in the simulation deck to model the substrate contacts that were employed in the measured test structures. This contact was spaced several microns from the active device, similar to the physical test structures irradiated in this study. Top side contacts are predominantly used with commercial SiGe foundry processes so that resistive losses in the bulk silicon are minimized for a given applied substrate potential (arising from the low doped, $\sim 10^{15}$ cm^{-3}, high resistivity substrates). The ion strike simulations were performed using an ion LET of 7 MeV $\mathrm{cm}^2/\mathrm{mg}$ and a penetration depth of 25.4 μm in the bulk silicon (calculated in SRIM using the front side metal stack thickness [16]), roughly modeling the ^{16}O ion used at SNL. The strike location was chosen to be through the N-Ring, external to the trench isolation of the device. The biases on the emitter, substrate, and base were fixed at ground (given that external trench responses will only be dictated by the collector, substrate and N-Ring), while the N-Ring was held at 3.3 V. Multiple simulations were run with varying collector voltages (0 V, 1.0 V, and 3.3 V) in order to determine the bias dependence of the transient response. In Fig. 8 and Fig. 9 the transients induced on all terminals for a device with a collector held at 0 V and 3.0 V, respectively, are plotted as a function of time. For NanoTCAD, the polarity of terminal currents is determined by the current directionality at the model interfaces, with positive current indicating current flowing out of the 3-D model boundary and negative flowing into the model boundary.

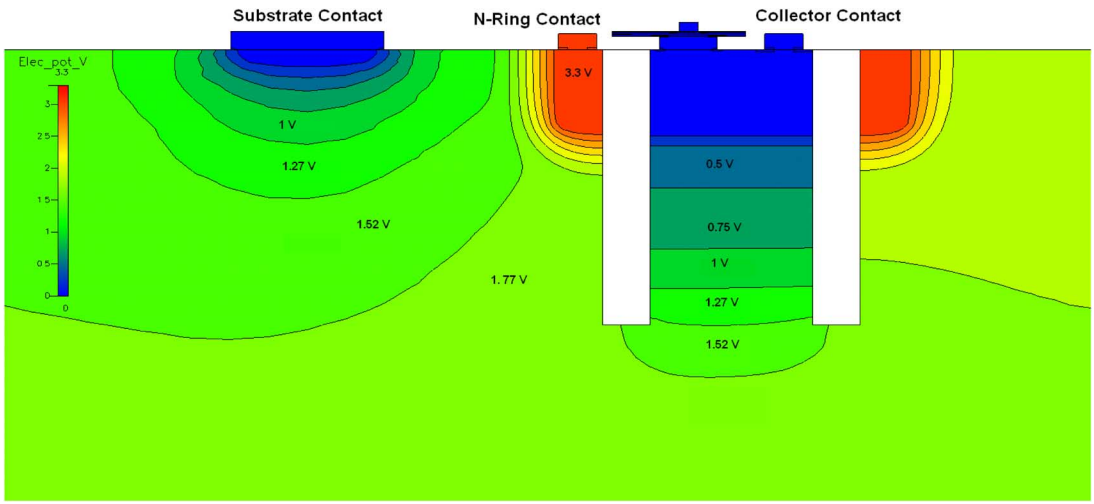

Fig. 11. Cross-sectional view of an N-Ring HBT showing the potential contours through the substrate occurring 0.86 ns after an N-Ring centered strike.

Given this standard it is understood that directly following the ion strike, current flows out of the collector terminal of the device (analogous to electrons flowing into the collector terminal). Near the conclusion of the transient signal, however, the polarity is swapped as current flows into collector (electrons flowing out of the terminal). In order to analyze the transient response, it is necessary to break the signal into different regions. The presence of these regions in the transient signature is dependent on terminal biases, as can be observed by comparing Fig. 8 and Fig. 9.

A. Region 1

The first region of the transient waveform occurs nearly instantaneously following the ion strike and is essentially identical between both collector bias conditions. As the ion passes through the semiconductor material, it ionizes a dense concentration of electron-hole pairs. The charge carriers ionized within the depletion region of the N-Ring-substrate junction are separated by the electric field. Electrons are pulled out of the N-Ring contact while holes are dumped into the lightly doped substrate. These excess holes begin to diffuse to the subcollector-substrate junction and accumulate, as they are pushed back by the electric field of this junction. This junction acts as a capacitor, balancing the gathering positive charges by pulling electrons into the 3-D model from the collector contact to the collector side of the subcollector-substrate junction. In Fig. 10, the time evolution of the build-up of excess free carriers is plotted along a vertical slice through the device. The number of excess carriers is calculated by the difference in carrier concentration at steady state prior to the strike, and at a given time step. Given how quickly the carrier interaction occurs within this region ($\sim$10 ps), the measurement set-up will be unable to capture this transient response since the sampling rate of the oscilloscope is limited to 20 ps/sample.

B. Region 2

The transient shifts from region 1 to region 2 as the substrate potential sufficiently modulated to turn on the parasitic NPN transistor formed by the N-Ring-substrate-collector. This process has been termed "funneling" in the literature and describes the collapse of a junction as a result of a sudden flood of free charge carriers and the subsequent push-out of electric field lines (potential gradient) to maintain the fixed voltage drop applied to contacts [20], [21]. In this case, the N-Ring-substrate junction collapses as a result of an ion strike, raising the potential of the bulk substrate. In Fig. 11 a cross-section of the modeled device displays the potential contours through the substrate, at a time corresponding to the peak collector current induced within region two (0.86 ns) of Fig. 9. At this point, the substrate potential has been raised such that the subcollector-substrate junction becomes forward biased, acting as the emitter-base junction of the parasitic bipolar transistor. A forward current of electrons flows from the collector to the N-Ring terminal until the N-Ring-substrate junction re-establishes itself, lowering the substrate potential and turning off the parasitic device. This region of the transient signal is highly dependent on the terminal biases, as reflected in Fig. 8 and Fig. 9. If a sufficient reverse-voltage bias is applied to the collector-substrate junction, the potential modulation of the substrate will not be sufficient to forward-bias this junction to turn the parasitic NPN transistor on.

C. Region 3

In the final region of the transient, the polarity of the collector signal flips. Electrons which have been ionized deep in the lightly doped substrate have now diffused from the strike path and reached the subcollector-substrate junction. With the substrate only doped on the order of 10^{15} $\mathrm{dopants/cm^3}$, free carriers are able to diffuse nearly 100 μm before experiencing recombination events. As electrons are impingent on the depletion region boundary they are swept across by the electric field and pulled out of the collector terminal.

V. Discussion and Summary

The impact of N-Rings on SiGe HBTs has been fully explored, uncovering the complex transient responses and bias dependencies. By collapsing the data taken from both the analog

and digital circuit experiments as well as the single-device measurements, some significant conclusions can be drawn, with impact on design of radiation tolerant SiGe circuits. It has been shown that reductions in peak transient pulses can be achieved by trading off an increase in SET sensitive volume (increase in small amplitude transients) for the analog design case of the voltage regulators [8], thereby providing potential benefit to applications that have failure criteria for voltage disturbances beyond a critical value. However, with judicial placing of N-Ring SiGe HBTs within the voltage reference, reductions in peak amplitude can be achieved without the addition of new small transients. This can be seen from the previous results [8], where only certain banks of transistors would show a response to ion strikes through the N-Ring region. Determining which transistor within an analog topology benefits from using an N-Ring SiGe HBT is not a simple task and requires the heavy computational burden of mixed-mode simulations.

For the case of the digital circuits (two 16-bit shift registers), it has been shown that single and multiple bit upsets are increased when incorporating N-Ring SiGe HBTs into the latch architecture. Typically, for ion-strikes to an HBT, the HBT collector sinks transient current, resulting in the pulling of nodes from a high potential to a lower one (often denoted as altering a digital state "1" to a digital state "0"). For the case of the N-Ring SiGe HBT, if an ion strikes through the N-Ring terminal, the HBT collector will source current, raising the nodal potential. An additional mode of latch upset is now introduced, with the possibility of a digital "0" becoming a digital "1" after a strike. As is reflected in the error cross-section measurements, this will result in nearly double the errors for an N-Ring HBT register. Consequently, the impact of incorporating N-Ring HBTs into circuit designs is strongly dependent on circuit topology (e.g., analog vs. digital), the important failure modes, and overall system sensitivity.

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