The Effects of Proton Irradiation on the Performance of High-Voltage n-MOSFETs Implemented in a Low-Voltage SiGe BiCMOS Platform

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***Abstract*—This paper presents the first comprehensive investigation of the impact of proton irradiation on the performance of high-voltage (HV) nMOS transistors implemented in a low-voltage (LV) SiGe BiCMOS technology. The effects of irradiation gate bias, irradiation substrate bias, and operating substrate bias on the radiation response of these transistors are examined. Experimental results show that the radiation-induced subthreshold leakage current under different irradiation biasing conditions remains negligible after exposure to a total dose of 600 krad(Si). We find that there are differences in the radiation response of LV and HV MOSFETs, suggesting that the mechanisms involved in causing degradation in LV and HV transistors could be of fundamentally different origins.**

***Index Terms*—High-voltage CMOS transistors, ionization damage, MOSFET, SiGe, total dose radiation effects.**

I. Introduction

SILICON-GERMANIUM (SiGe) BiCMOS technology has emerged as a compelling technology platform for implementing mixed-signal electronic circuits intended for extreme environment applications. The heterojunction bipolar transistors (HBTs) in SiGe technology offer transistor-level performance metrics comparable with those of III-V devices while maintaining much higher levels of integration, yield, and reliability. In addition, *dc* and *ac* performance metrics of these bandgap-engineered transistors naturally improve with cooling [1], [2]. SiGe HBTs have also a desirable side benefit of possessing an inherent hardness to ionizing radiation, immunity to enhanced low dose rate sensitivity (ELDRS), and have been shown to be total ionization dose (TID) tolerant down to 77 K operating temperatures to multi-Mrad levels [3]. These unique features of SiGe HBTs make SiGe technology a strong candidate for extreme environment applications such as unmanned missions to the lunar surface, a classical example of an extreme environment. The ambient temperature on the Moon ranges from $+120°C$ (in the sunshine) to $-230°C$ (in the shadowed polar craters), and the surface of the Moon is exposed to both cosmic rays and solar events, creating significant single event effect (SEE) hazards, as well as modest levels of total dose. Implementation of mixed-signal circuits capable of operating reliably under lunar extreme environment conditions will eliminate the need for shielded "warm boxes" (the current practice) and therefore, can greatly improve system performance, decrease weight, and increase the reliability of the overall mission.

Aside from SiGe HBTs, unmanned robotic space missions require high-voltage (HV) transistors (e.g., 20 V) for use in motor actuators and input/output interface circuits. In order to have a low cost and fully integrated system-on-a-chip for space missions, it is desirable to have these HV transistors fabricated on the same substrate as the low-voltage (LV) SiGe HBTs and MOSFETs (e.g., 3.3 V). The integration of HV transistors within existing LV processes has been a topic of significant interest for decades [4]–[9]. In general, HV operation in a standard process is achieved by using either circuit or device techniques [5]. Circuit techniques usually involve cascading LV transistors to effectively achieve HV operation. This approach, however, increases the circuit complexity and the required power to maintain intermediate voltages for gate drive [9]. Among the proposed device techniques, lateral double-diffused MOS (LDMOS) and drain-extended MOS (DEMOS) structures are the most popular solutions for fabricating HV transistors on the same substrate as LV transistors. LDMOS devices require extra masks and processing steps [6], while DEMOS transistors are relatively easy to fabricate, since they share the same uniformly doped channel with their LV counterparts [7]. Before these HV devices can be used on long-term space missions, however, their performance under extreme environment conditions (over wide temperature range and under radiation exposure) needs to be thoroughly evaluated. In addition, the operative damage mechanisms involved in causing possible performance degradation under such extreme conditions must be understood. In terms of radiation response of HV transistors, very little information exists [10]–[12]. The work in [10], [11] has focused on the radiation response of LDMOS transistors

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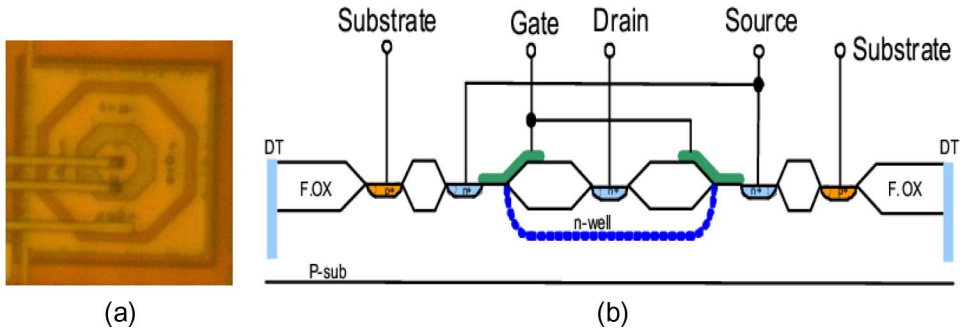

Fig. 1. (a) Layout and (b) cross-section of a HV nMOS transistor implemented in first-generation SiGe BiCMOS platform.

implemented in SOI and SIMOX platforms, respectively, while in [12] we have very briefly discussed the preliminary response of a prototype HV transistor implemented in a SiGe technology.

This paper presents, for the first time, a comprehensive investigation of the impact of proton irradiation on the performance of HV transistors implemented in a first-generation, commercially-available 3.3 V SiGe technology. HV transistors were irradiated under several different biasing conditions. Experimental results are presented and the results are discussed. Differences in the radiation response of the HV and LV transistors are highlighted. These differences suggest that the degradation mechanisms involved in LV and HV transistors could be of fundamentally different origins and thus motivate further in-depth investigation.

II. Process Technology and HV Devices

For the present study, HV transistors were implemented in a first-generation 3.3 V SiGe BiCMOS technology (IBM's SiGe 5AM) platform by employing special layout techniques. No process changes were made to the technology and no additional mask layers were utilized. IBM's SiGe 5AM technology is a four-level metal process and features SiGe HBTs with an emitter width of 0.5 μm and a unity gain cut-off frequency and maximum frequency of oscillation of 45 GHz and 60 GHz, respectively, offering more than adequate performance for the intended lunar applications; nMOS and pMOS transistors with a nominal L_{eff} of 0.35 μm, as well as polysilicon and diffused resistors, and various capacitors.

Avalanche breakdown located at the edge of the drain is the primary factor in limiting the voltage blocking capability of the conventional nMOS transistors [7]. To build HV transistors compatible with standard LV transistors new device structures must therefore be created. Layout and cross-section of such a HV transistor is shown in Fig. 1. This device is based upon a conventional n-channel MOSFET with the drain area surrounded by an n-well. The n-well is used to define the lightly doped n-type "drift" region [7]. Since the n-well has a low surface doping level, the surface electric field is decreased, resulting in a device with a high breakdown voltage. Three independent layout parameters; namely, the channel length, the gate overlap of the drift region, and the length of the lightly doped drift region, can influence the performance, the breakdown voltage, and the reliability lifetime characteristics of this HV transistor, and thus need to be carefully addressed [13]. The transistors chosen for this study have a gate length of 2 μm and gate width of 40 μm. With the drift region length of 4.35 μm, a blocking voltage of 57 V was achieved, which is more than adequate for the intended application.

III. Experiment

63 MeV proton irradiation was performed at the Crocker Nuclear Laboratory at the University of California at Davis, at a dose rate of 1 krad(Si)/s. The dosimetry measurements used a five-foil secondary emission monitor calibrated against a Faraday cup, and Ta scattering foils located several meters upstream of the target establish a beam spatial uniformity of 15% over a 2.0 cm radius circular area. The dosimetry system has been previously described [14], and is accurate to about 10%.

A total number of fourteen HV transistors with $(W/L) = 40\ \mu\mathrm{m}/2\ \mu\mathrm{m}$ from two fabrication experiments were mounted in 28-pin DIP ceramic packages, wire-bonded, and extensively characterized before being irradiated. Since these devices were designed by manipulating their layout and intentionally violating selected design rules, variations among different transistor designs are expected. Irradiation was performed at room temperature and under different biasing conditions. At least two samples were considered for each irradiation experiment. Post-irradiation measurements were performed two weeks after irradiation. Experiments and results are discussed in the following section.

IV. Results and Discussion

Fig. 2 shows the subthreshold characteristics of a HV nMOS transistor with $\mathrm{W/L} = 40\ \mu\mathrm{m}/2\ \mu\mathrm{m}$, measured at $V_{\mathrm{DS}} = 10.05$ V and at four different temperatures. Similar to LV nMOS transistors, the subthreshold slope and the threshold voltage increase and the subthreshold leakage decreases as the temperature is reduced. The transistor exhibits a zero temperature coefficient bias point in the vicinity of the gate-source voltage of 1.1 V. The output characteristics of the same HV transistor measured at two gate-source voltages and at four different temperatures are shown in Fig. 3. The drain current and the output conductance in the saturation region increase as the temperature decreases, similar to what is expected from LV nMOS transistors [15]. Observe that, at a certain temperature, the output conductance is negligible for $V_{\mathrm{DS}} < 20$ V but increases beyond $V_{\mathrm{DS}} = 20$ V. To gain more insight into this, the drain current and the absolute values of the source and the substrate currents

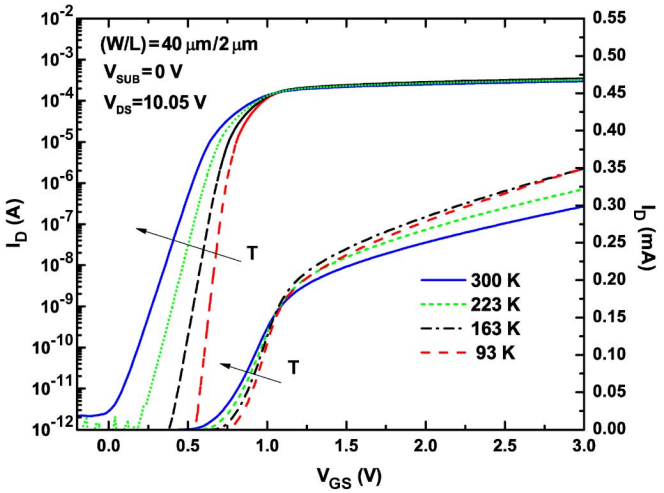

Fig. 2. $I_D - V_{GS}$ characteristics of a HV nMOS transistor as a function of temperature.

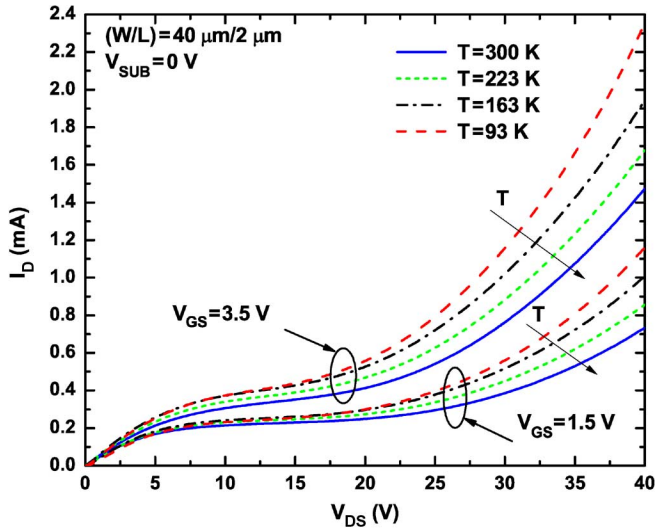

Fig. 3. $I_D - V_{DS}$ characteristics of a HV nMOS transistor as a function of temperature.

at two temperatures are plotted in Fig. 4. As can be seen, the substrate current starts to increase for $V_{DS} > 20$ V (onset of impact ionization). The increase in the output conductance at high drain voltages has been also observed in HV transistors fabricated in technologies other than SiGe technology [5], [9].

Figs. 2 and 3 verify that these HV transistors can reliably function in the range of $V_{DS} < 20$ V to temperatures as low as 93 K, the intended application in this case. To ensure the extreme environment capability of these transistors, in addition to their cryogenic performance, their radiation response needs to be thoroughly studied. Proton irradiation was performed under three different biasing conditions: 1) irradiation with all pins grounded, 2) irradiation under gate bias, and 3) irradiation with biased gate and substrate. The impact of operating substrate bias was also investigated. The following sections present the experimental results from each radiation experiment.

A. Irradiation With All Pins Grounded

Fig. 5 depicts the $I_D - V_{GS}$ characteristics for a HV transistor irradiated with all pins grounded, as a function of equivalent total dose. The characteristics were measured at $V_{SUB} =$

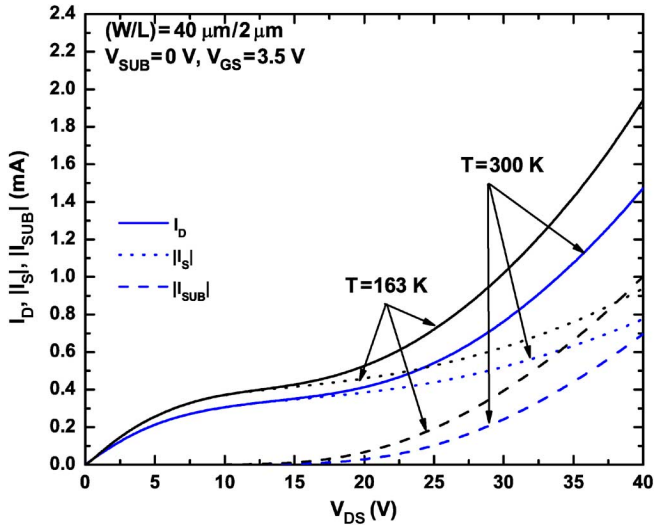

Fig. 4. I_D, $|I_S|$, and $|I_{SUB}|$ as a function of V_{DS} for a HV nMOS transistor at two temperatures.

0 V and $V_{DS} = 5.05$ V. The degradation in the threshold voltage is negligible after irradiation, as expected. Similar to LV NMOS transistors, the off-state leakage increases after irradiation. Interestingly, however, the increase in the leakage current remains below 100 pA, even after exposure to total ionization dose level of 600 krad(Si). It was observed that the leakage current in LV NMOS transistors in this SiGe technology increases to about 10 μA after irradiation to TID level of only 100 krad(Si) [16]. In LV NMOS transistors, typically two radiation-induced leakage mechanisms are responsible for causing the subthreshold leakage current. One mechanism, known as Gate-Induced-Drain-Leakage (GIDL), is the radiation-induced tunneling (band-to-band and/or trap-assisted) in the gate-to-drain overlap region [17], [18] which causes a negative slope in the drain current in $V_{GS} < 0$ region. As the gate bias voltage is reduced, the junction field is increased, causing the minority carriers to be swept away into the substrate and resulting in an increase in the leakage current. The other cause of subthreshold leakage current is the presence of radiation-induced positive charges in the region where the gate extends over the shallow trench isolation (STI) edge, effectively creating a shunt leakage path from source-to-drain. This will result in a positive sloping drain current in the negative gate-source voltage region [19]. As seen from Fig. 5, none of the two mentioned radiation-induced LV damage mechanisms are significantly involved in the operation of HV transistor, and the subthreshold leakage current does not increase substantially after irradiation. For a better understanding, the substrate current was also measured at each dose level and is plotted in the same figure. As can be seen, the substrate current level remains less than 10 pA after irradiation to total dose level of 600 krad(Si) and does not show any significant dependence on GIDL or STI edge leakage. The differences in the radiation response of LV and HV transistors could be the result of differences in their layout structures. Further investigation is required to fully understand these differences and will be reported at a later date.

Fig. 6 shows the $I_D - V_{DS}$ characteristics of the same transistor measured at $V_{SUB} = 0$ V and $V_{GS} = 1$ V and $V_{GS} =$

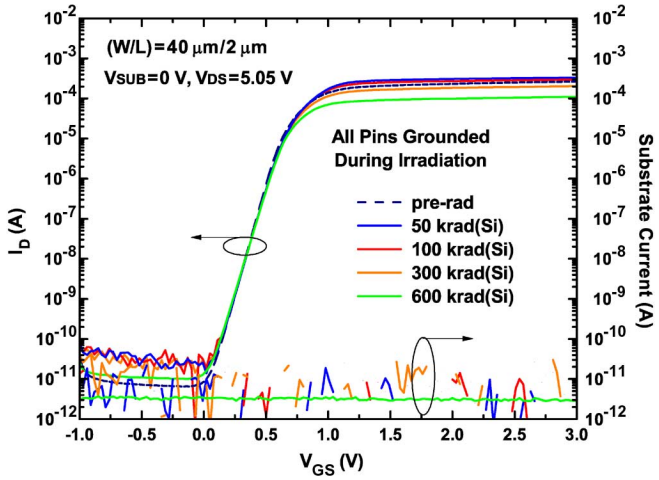

Fig. 5. $I_D - V_{GS}$ and $I_{SUB} - V_{GS}$ characteristics of a HV nMOS transistor as a function of dose for irradiation with all pins grounded.

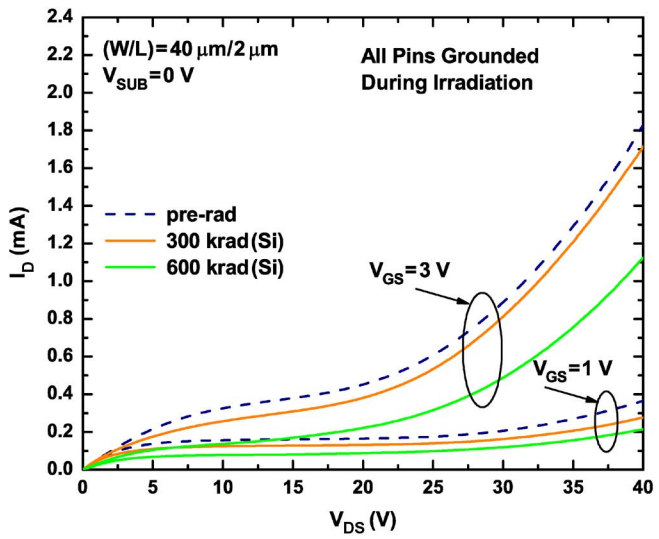

Fig. 6. $I_D - V_{DS}$ characteristics of a HV nMOS transistor as a function of dose for irradiation with all pins grounded.

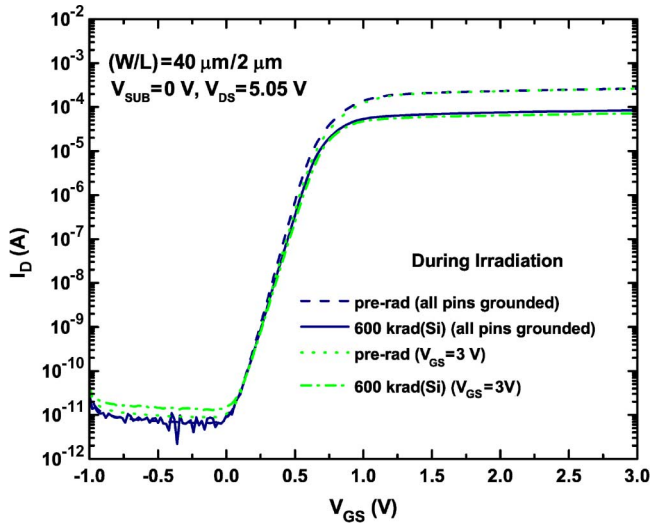

Fig. 7. $I_D - V_{GS}$ characteristics of HV nMOS transistors for $V_{GS} = 3$ V and 0 V irradiation conditions.

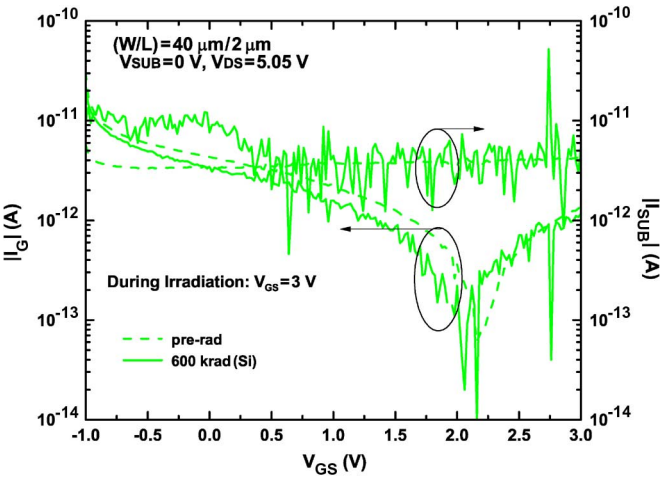

Fig. 8. $|I_G|$, and $|I_{SUB}|$ characteristics of a HV nMOS transistors for $V_{GS} = 3$ V irradiation condition.

3 V. It is well known that the mobility of carriers is degraded as radiation dose is increased, and as a result the current drive capability of the transistors is reduced [20]. It can be seen from Fig. 6 that as soon as the transistor turns on, the drain current decreases after irradiation. The reduction in the drain current is more significant when the transistor is exposed to 600 krad(Si). This post-rad degradation can also be observed in the on-regime part of Fig. 5. As discussed above, this degradation could be attributed to the decrease in the effective channel mobility after radiation. Similar post-rad current drive capability degradation was observed in power MOSFETs [21].

B. Effect of Irradiation Gate Bias

It is well known that gate bias during irradiation significantly increases the leakage current in LV nMOS transistors [22]. To investigate the impact of irradiation gate bias on the DC performance of HV nMOS transistors, HV transistors were irradiated at the gate bias of 3 V to total equivalent dose level of 600 krad(Si). The substrate voltage was set to ground during the irradiation. $I_D - V_{GS}$ characteristics were measured for $V_{DS} = 5.05$ V and the results are plotted in Fig. 7. Measurement results from grounded irradiation experiment are also included for ease of comparison. The figure shows that the increase in the subthreshold leakage current for $V_{GS} = 3$ V irradiation is slightly higher than for $V_{GS} = 0$ V irradiation. However, the leakage remains below 100 pA, which is acceptable for circuit operation, without employing any radiation hardening techniques. In order to gain more insight for the involved degradation mechanisms, the absolute values of the substrate and gate currents are plotted as a function of V_{GS} in Fig. 8. As can be seen, there is negligible change in the gate current after irradiation. However, the substrate current increases after irradiation under gate bias (as expected) and this attributes to the slight increase in the subthreshold leakage current.

Fig. 9 shows the $I_D - V_{DS}$ characteristics of two HV transistors, one irradiated with all pins grounded and one irradiated under applied gate bias, measured at 0 V operating substrate and $V_{GS} = 1$ V and $V_{GS} = 3$ V. It can be seen that the drain current

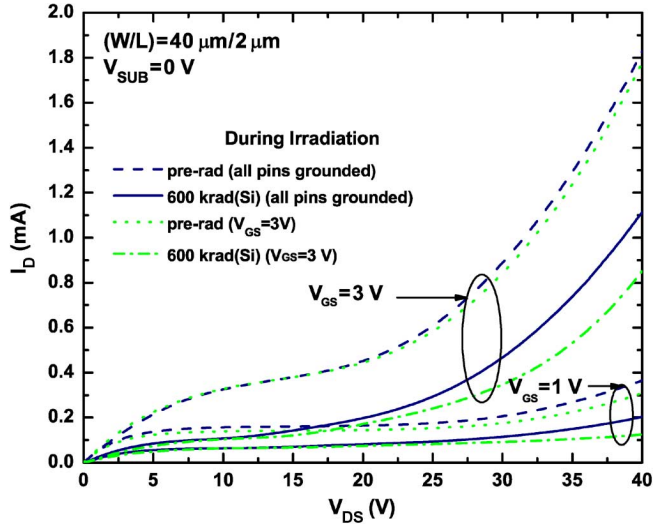

Fig. 9. $I_D - V_{DS}$ characteristics of HV nMOS transistors for $V_{GS} = 3$ V and 0 V irradiation conditions.

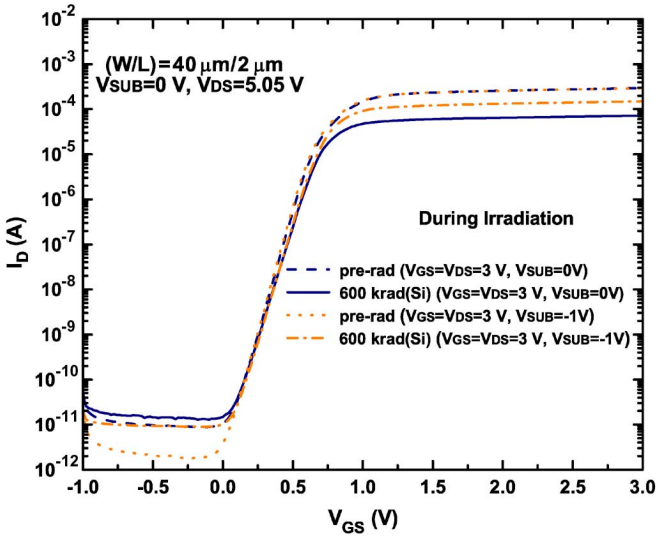

Fig. 10. $I_D - V_{GS}$ characteristics of HV nMOS transistors for irradiation substrate bias of 0 V and -1 V.

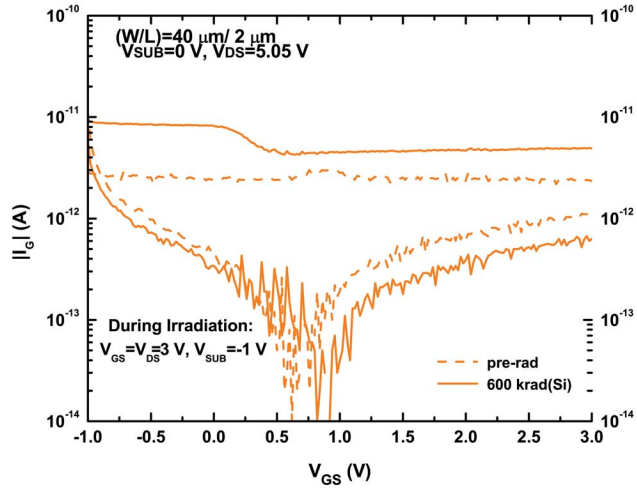

Fig. 11. $|I_G|$, and $|I_{SUB}|$ characteristics of a HV nMOS transistors for $V_{GS} = V_{DS} = 3$ V and $V_{SUB} = -1$ V irradiation condition.

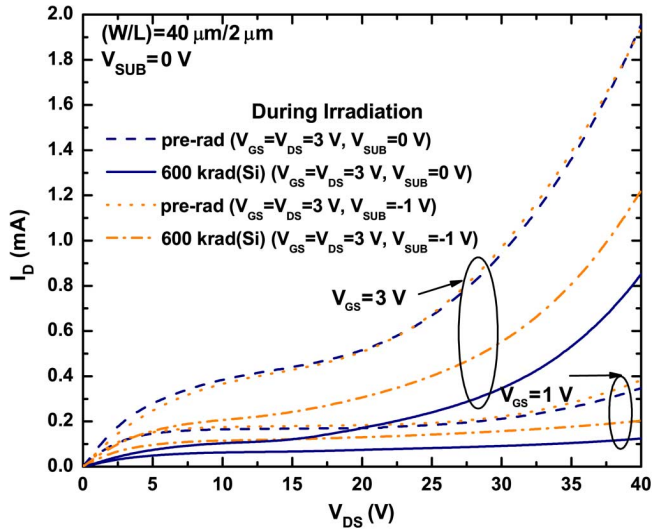

Fig. 12. $I_D - V_{DS}$ characteristics of HV nMOS transistors for irradiation substrate bias of 0 V and -1 V.

decreases after irradiation. This degradation is more significant at $V_{GS} = 3$ V for the gate-bias irradiation. This degradation in the current drive capability, again, can be attributed to the degradation in the effective channel mobility.

C. Effect of Substrate Bias During Irradiation

To investigate the impact of substrate bias during irradiation, HV transistors were irradiated under $V_{GS} = V_{DS} = 3$ V and with 0 V and -1 V substrate bias conditions. Fig. 10 illustrates $I_D - V_{GS}$ characteristics from this experiment measured at 0 V substrate voltage and $V_{DS} = 5.05$ V. Observe that the increase in the leakage current is higher for the transistor irradiated at -1 V substrate voltage than for the one irradiated at 0 V substrate voltage. The increase in the subthreshold leakage after irradiating the transistor under negative substrate voltage is consistent with what has been observed in LV NMOS transistors [19]. However, the level of radiation-induced leakage current in these HV transistors is significantly smaller than that of LV transistors as the leakage current remains below 100 pA. The absolute values of the substrate and gate currents are plotted in Fig. 11 as a function of gate-source voltage. Slight increase in the substrate current is observed after irradiation, which results in an increase in the subthreshold leakage current. The gate current slightly decreases after irradiation.

$I_D - V_{DS}$ characteristics of HV transistors irradiated under substrate voltages of 0 V and -1 V are shown in Fig. 12. Output characteristics are measured at $V_{GS} = 1$ V and $V_{GS} = 3$ V. As can be seen, the current drive capability has been less degraded after irradiation with negative substrate bias.

D. Effect of Substrate Bias During Normal Operation Post Irradiation

It is has been previously shown that negative operating substrate bias can suppress the radiation-induced STI subthreshold leakage in LV nMOS transistors [19]–[22]. To examine the effects of negative substrate bias operation on the performance

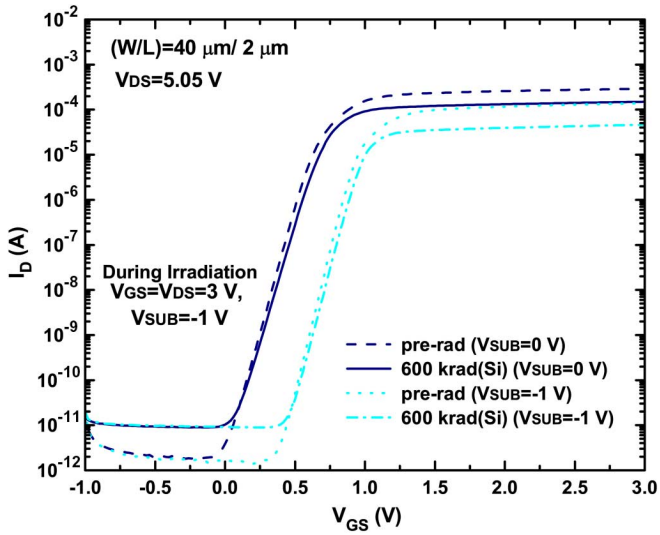

Fig. 13. Comparison of $I_D - V_{GS}$ characteristics of a HV nMOS transistor for operating substrate bias of 0 V and -1 V. The irradiation bias conditions were $V_{GS} = V_{DS} = 3$ V and $V_{SUB} = -1$ V.

of HV nMOS transistors, $I_D - V_{GS}$ characteristics of a transistor irradiated under $V_{GS} = V_{DS} = 3$ V and $V_{SUB} = -1$ V were measured at a substrate potential of both 0 V and -1 V. Measurement results are plotted in Fig. 13. Contrary to what is expected in LV transistors, no significant improvement was observed in the post-radiated subthreshold leakage current of HV transistors when a negative voltage is applied to the substrate.

V. Summary

We have presented experimental results of the effects of proton irradiation on the performance of high-voltage (HV) nMOS transistors implemented in a low-voltage (LV) SiGe BiCMOS technology. The impact of irradiation gate bias, irradiation substrate bias, and operating substrate bias on the radiation tolerance of these transistors was investigated. It was shown that the radiation-induced subthreshold leakage current of these HV transistors, under different irradiation biasing conditions, remains below 100 pA to 600 krad, clearly good news for circuits required for unmanned space missions. It was observed that the level of radiation-induced leakage current in the HV transistors is significantly smaller than that of LV transistors. A careful comparison of the radiation response of HV transistors and their LV counterparts reveals there are some significant differences in their radiation responses, which suggests that the mechanisms involved in causing degradation in LV and HV transistors could be of fundamentally different origins and therefore require further investigation.

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