Application of RHBD Techniques to SEU Hardening of Third-Generation SiGe HBT Logic Circuits

Ramkumar Krithivasan, Paul W. Marshall, Mustayeen Nayeem, Akil K. Sutton, Wei-Min Kuo, Becca M. Haugerud, Laleh Najafizadeh, John D. Cressler, Martin A. Carts, Cheryl J. Marshall, David L. Hansen, Kay-Carol M. Jobe, Anthony L. McKay, Guofu Niu, Robert Reed, Barbara A. Randall, Charles A. Burfield, Mary Daun Lindberg, Barry K. Gilbert, and Erik S. Daniel

***Abstract*—Shift registers featuring radiation-hardening-by-design (RHBD) techniques are realized in IBM 8HP SiGe BiCMOS technology. Both circuit and device-level RHBD techniques are employed to improve the overall SEU immunity of the shift registers. Circuit-level RHBD techniques include dual-interleaving and gated-feedback that achieve SEU mitigation through local latch-level redundancy and correction. In addition, register-level RHBD based on triple-module redundancy (TMR) versions of dual-interleaved and gated-feedback cell shift registers is also realized to gauge the performance improvement offered by TMR. At the device-level, RHBD C-B-E SiGe HBTs with single collector and base contacts and significantly smaller deep trench-enclosed area than standard C-B-E-B-C devices with dual collector and base contacts are used to reduce the upset sensitive area. The SEU performance of these shift registers was then tested using heavy ions and standard bit-error testing methods. The results obtained are compared to the unhardened standard shift register designed with CBEBC SiGe HBTs. The RHBD-enhanced shift registers perform significantly better than the unhardened circuit, with the TMR technique proving very effective in achieving significant SEU immunity.**

***Index Terms*—Current mode logic (CML), heavy ion, heterojunction bipolar transistor (HBT), radiation hardening by design (RHBD), shift register, silicon-germanium (SiGe), single-event upset (SEU), triple-module redundancy (TMR).**

I. Introduction

SILICON-GERMANIUM (SiGe) heterojunction bipolar transistor (HBT) technology has generated considerable interest in the space community due to its robustness to total ionizing dose (TID) radiation, without any additional hardening [1]. This TID tolerance does not, unfortunately, translate into improved single event upset (SEU) response for SiGe HBT logic. Digital circuits designed in first-generation (50 GHz) and second-generation (120 GHz) SiGe technology have been shown to be very sensitive to SEU [2]–[5], and circuit-level hardening using the current-shared hardening (CSH) [6] technique proved ineffective in mitigating single event upsets in these circuits.

Radiation-hardening-by-design (RHBD) employs layout and circuit architecture changes for the radiation hardening of space electronic systems using commercial foundry processes, with no modifications to the existing process or violation of design rules. In this work, we have applied RHBD techniques to improve the SEU immunity of SiGe HBT high-speed logic circuits.

II. SiGe HBT BiCMOS Technology

Shift registers featuring these RHBD techniques were realized for the first time in the commercially-available IBM SiGe 8HP BiCMOS technology platform. This process incorporates a 130 nm "raised extrinsic base" SiGe HBT structure with an *in-situ* doped polysilicon emitter, deep and shallow-trench isolation. The SiGe HBT has a peak unity-gain cut-off frequency (f_T) of 200 GHz [7]. The technology also integrates 130 nm CMOS devices as well as a wide array of passive elements and seven layers of metalization.

III. SiGe RHBD Techniques

A. Circuit-Level Techniques

Three different types of 16-bit shift registers in the current mode logic (CML) family were investigated in this work. The clock "tree" architecture in these shift registers was identical to the one used in shift registers reported in [3], with a master clock buffer driving four intermediate clock buffers, each in turn providing clock inputs to a set of 4-D flip flops (Fig. 1). Thus, as was noted in [3], an upset occurring in the clock tree has the potential to cause multiple bit upsets. Therefore, to improve their SEU immunity, the clock buffers in the present designs featured circuit-level hardening based on the gated-feedback cell (GFC) RHBD technique [8]. Two RHBD local circuit-redundancy based circuit-level hardening techniques were employed in the design of the constituent D-flip flops in two of the three shift registers, while the remaining shift register, referred to as "standard MS SR" ("std. SR"), featured unhardened conventional CML master-slave (MS) D-flip flops (Fig. 2), and was

Manuscript received July 14, 2006; revised August 21, 2006. This work was supported by the DARPA RHBD Program, DTRA under the Radiation Hardened Microelectronics Program, NASA-GSFC under the NASA Electronic Parts and Packaging (NEPP) Program, Mayo Foundation, Boeing, NASA ETDP, and the Georgia Electronic Design Center at Georgia Tech.

R. Krithivasan, M. Nayeem, A. K. Sutton, W.-M. L. Kuo, B. M. Haugerud, and J. D. Cressler, are with the School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA 30332 USA (e-mail: ramkumar@ece.gatech.edu).

P. W. Marshall is with NRL/NASA, Brookneal, VA 24528 USA.

M. A. Carts and C. J. Marshall are with the NASA Goddard Spaceflight Center, Greenbelt, MD 20771 USA.

D. L. Hansen, K.-C. M. Jobe, and A. L. McKay are with the Boeing Space and Intelligence Systems, Los Angeles, CA 90009 USA.

G. Niu is with Auburn University, Auburn, AL 36849 USA.

R. A. Reed is with Vanderbilt University, Nashville, TN 37235 USA.

B. A. Randall, C. A. Burfield, M. D. Lindberg, B. K. Gilbert, and E. S. Daniel are with the Mayo Foundation, Rochester, MN 55901 USA.

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TNS.2006.885379

0018-9499/$20.00 © 2006 IEEE

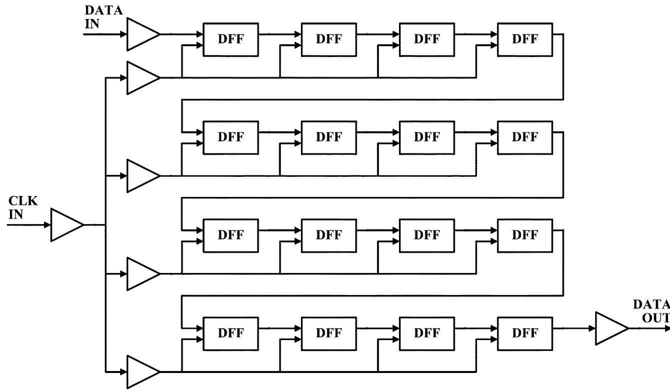


Fig. 1. Block diagram of the 16-bit shift registers.

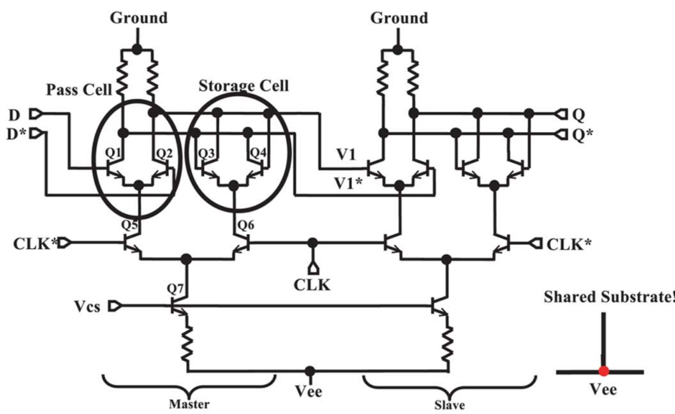


Fig. 2. Schematic of standard CML master-slave D-flip flop.

used as the baseline circuit (control) to enable meaningful comparisons. To study the effects of reduced bias current on the SEU characteristics of the shift registers, low-power ($I_{\mathrm{tail}} = 0.5$ mA) and high-power ($I_{\mathrm{tail}} = 1.0$ mA) versions were implemented. I_{tail} is the tail current of any differential pair in the D-flip flops. Upon complete switching the current flowing through the load resistor connected to the ON transistor is very close to I_{tail}.

1) Dual-Interleaving-Based RHBD: One of the RHBD shift registers incorporated D-flip flops based on a newly proposed circuit implementation [10], referred to here as "dual-interleaved SR" or "DI SR" (Fig. 3). A previous study [11] on the dependence of SEU response on circuit architecture in the CML logic family indicated that cross-coupling at the transistor-level, required for the storage cell functionality in the standard master-slave D-flip flop (Fig. 2), increases the vulnerability of this circuit to SEU. Thus, local redundancy was built into the standard master-slave D-flip flop, which consumes the least power and occupies the smallest area, to incorporate limited transistor-level decoupling in the storage cell, thereby mitigating its SEU sensitivity with only a moderate increase in power consumption and circuit complexity.

Unlike the standard MS SR, the base and the collector of the transistors in the storage cell of the DI SR are not connected to the same differential pair in the pass cell, thus achieving effective decoupling of the base and collector terminals of the transistors in the storage cell. For instance, the base of Q5 in DI SR storage cell is connected to the collector of Q1 in the pass cell, whereas the collector of Q5 is connected to the collector of Q3 of the alternate differential pair in the pass cell. However, to maintain the storage cell functionality, the base and collector of each transistor in the storage cell are connected to complementary outputs from the pass cell. Thus, an SEU transient current flowing through the collector of the transistor Q5 does not affect the base directly. The voltage drop due to this transient flow, however, does affect the base of Q7, which might indirectly affect the base of Q5, potentially leading to upset [10].

2) Gated-Feedback Cell-Based RHBD: The other RHBD shift register featured a slightly modified gated-feedback cell (GFC) based master-slave D-flip flop [8], referred to here as "GFC SR" (Fig. 4). The OR-gates available in the GFC architecture perform a logical OR operation on identical logic outputs from the pass cell pair and feed the result back to the appropriate inputs of the duplicate storage cell pair. The OR operation, enabled by a pair of emitter followers, helps transmission of the correct logic to the storage cell inputs even when one of the OR gate inputs is in error via an ion strike.

The output of a two-input OR gate changes state only when both the inputs change state from high to low or low to high. A ion-strike on an npn transistor, in general, causes ion-induced current to flow into the collector, thereby pulling the collector potential low. Therefore, an ion strike on a storage cell transistor such as Q5 causes its collector and in turn the input to transistor Q9 to go low. This spurious transition, however, does not affect the output of the OR as the other input to Q10 is unaffected. In addition, the inputs to Q11 and Q12 (transistors in the alternate OR gate) are also unaffected, thereby ensuring the correct logic at the input (or base) of Q5. Thus, the OR-gate-based feedback to the storage cell inputs, in addition to local redundancy, is in principle expected to offer SEU immunity that is higher than that provided by dual-interleaving. In addition, there are diode voltage clamps positioned across the load resistors to increase the current onto an upset collector node, thus reducing the upset duration [8], [9].

3) Register-Level RHBD: Additional register-level RHBD based on triple-module redundancy (TMR) was applied to the low-power versions of DI SR and GFC SRs (referred to as DI TMR and GFC TMR, respectively), to gauge the performance improvement achieved from this additional level of RHBD. The output was selected based on majority voting between three redundant shift registers using GFC-hardened and unhardened voters working in parallel. Separate select lines (S1-S3) were provided for enabling or disabling individual shift registers in the circuit to test their functionality (Fig. 5).

B. Device-Level RHBD Techniques in SiGe HBTS

A previous microbeam study on second-generation SiGe HBTs concluded that the active region defined by the deep-trench (DT) boundary is only a portion of the upset sensitive volume and that the remaining sensitive volume encompasses the region of substrate several micrometers away from the trench [4]. Despite this observation, reduction in area enclosed by DT is expected to significantly improve the net upset cross-section of the transistor by reducing the effective

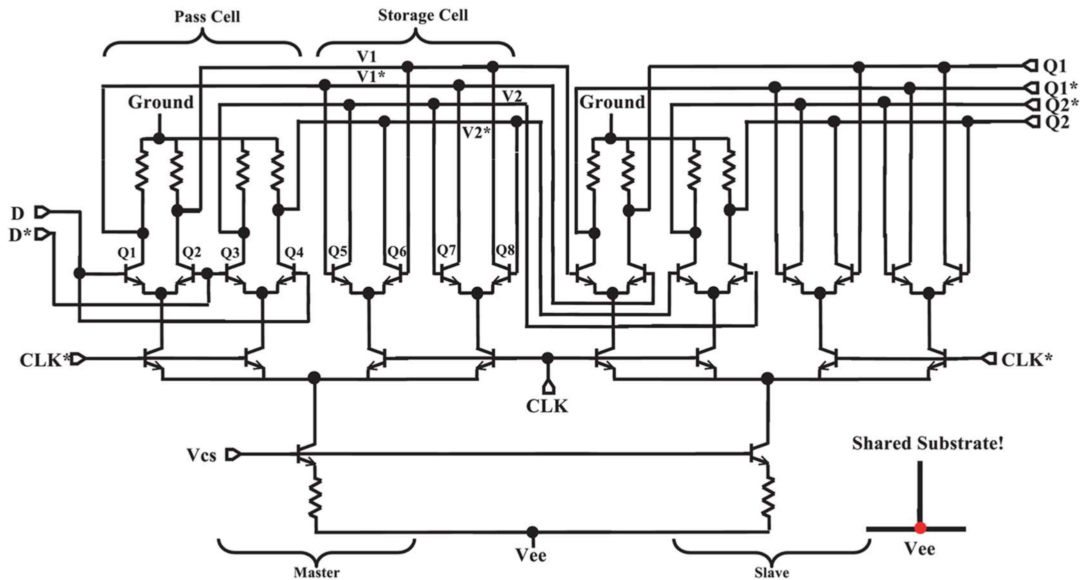


Fig. 3. Schematic of the new RHBD dual-interleaved D-flip flop circuit with minimal cross coupling in the storage cell.

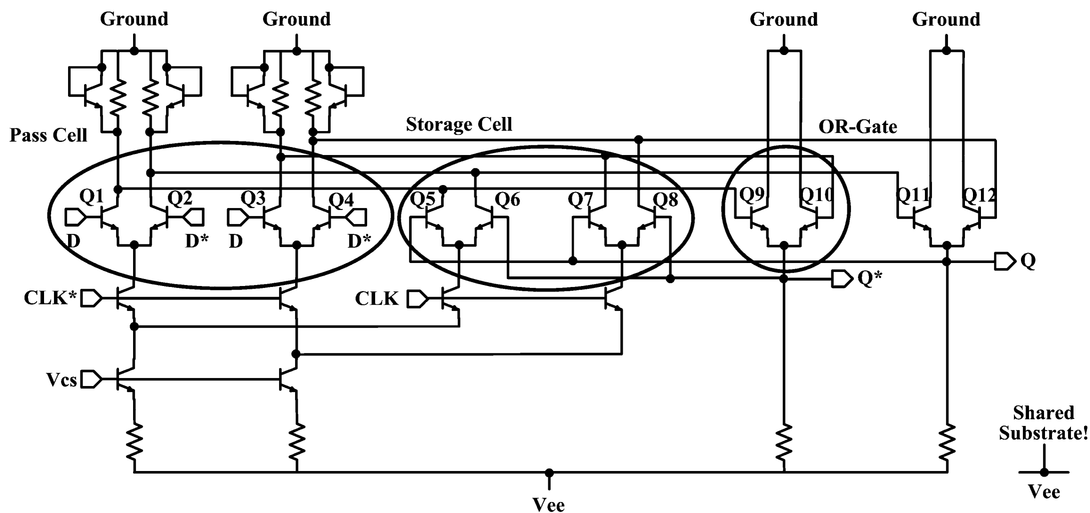


Fig. 4. Schematic of master stage of the GFC D-flip flop.

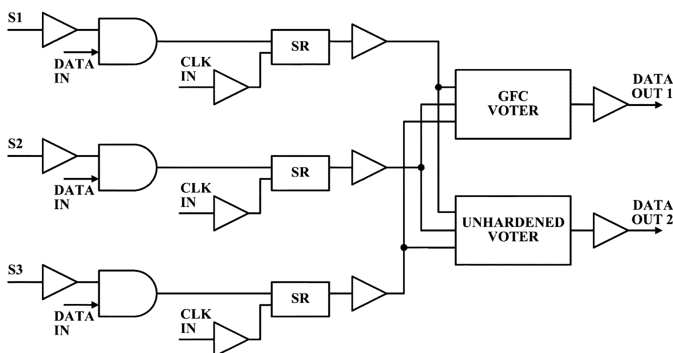


Fig. 5. Block diagram of the triple module redundancy (TMR) implementation.

sensitive area [12]. Thus, a transistor with minimum feature size, and with only a single collector, base, and emitter contacts (C-B-E), as opposed to the standard device with double collector and base contacts (C-B-E-B-C), was selected as the workhorse RHBD device to minimize local ion-induced upset cross-section within the RHBD latches. While the C-B-E-B-C device with an emitter area (A_E) of $0.12 \times 2.50\ \mu\text{m}^2$ was used in the baseline standard MS SR, the RHBD (C-B-E) device with A_E of $0.12 \times 0.52\ \mu\text{m}^2$ was employed in all other shift registers. Only a slight ac device performance penalty resulted. The internal trench area for the C-B-E-B-C was 15.10 μm^2 while that for the RHBD C-B-E devices was 4.08 μm^2. Thus, the net reduction in trench enclosed area for the RHBD SiGe HBT was about 73%. A bigger C-B-E-B-C device was intentionally used in the baseline circuit to demonstrate the degradation in upset cross-section associated with larger trench volume [Fig. 6(a) and (b)].

The various hardening techniques investigated are summarized in Table I. In addition, the total power consumption of the various shift registers, the contribution of individual D-flip flop to the total power consumption, the D-flip flop area, and the

TABLE I
COMPARISON OF HARDENING TECHNIQUES

Topology	Circuit Technique	Device Technique	
		Type	Emitter Area (μm^2)
Std SR	unhardened	C-B-E-B-C	0.12×2.50
DI SR	latch-level redundancy + limited decoupling	C-B-E	0.12×0.52
DI SR Low-P	latch-level redundancy + limited decoupling	C-B-E	0.12×0.52
DI TMR	three DI SR + voting at end	C-B-E	0.12×0.52
GFC SR	latch-level redundancy + OR-gate feedback + load diode clamps	C-B-E	0.12×0.52
GFC TMR	three GFC SR + voting at end	C-B-E	0.12×0.52

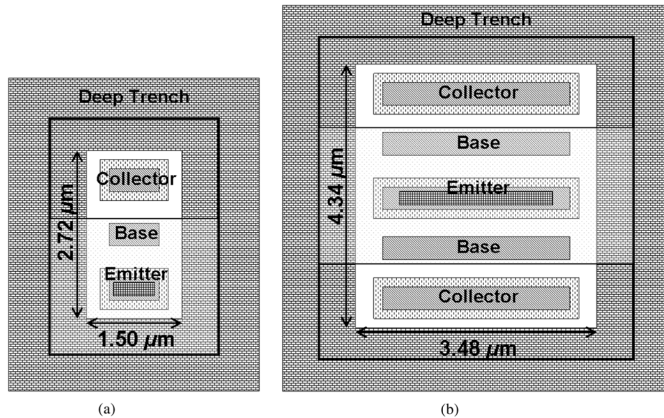


Fig. 6. (a) RHBD C-B-E transistor and (b) C-B-E-B-C transistor used in the baseline Std. SR.

maximum post-layout simulated speed are tabulated in Table II. Clearly, the operating speed of low power DI SR and the power consumption of its constituent D-flip flops are comparable with those of the standard SR with only a slight area penalty overhead and with minimal increase in layout complexity, suggesting that dual-interleaving can potentially be applied to other technology nodes. RHBD shift registers with much higher operating speeds than those presented here are clearly possible in this technology [13]. The primary reason for the more modest operating speeds for the present shift registers lies in the (intentional) overdesign of the latch output buffers, which caused significant internal capacitive loading. This can easily be altered as needed for specific speed requirements without compromising SEU performance. For instance, simulations using more standard buffers for the DI SR can be clocked to well above 20 GHz speeds. The die photomicrographs of a 16-bit shift register and its TMR implementation are shown in Fig. 7(a) and (b). The die area of 16-bit shift registers is 2.356×1.586 mm^2 and the die area of the TMR version is 2.636×2.686 mm^2, and dictated by the high-speed packaging fixture used.

IV. Test Setup

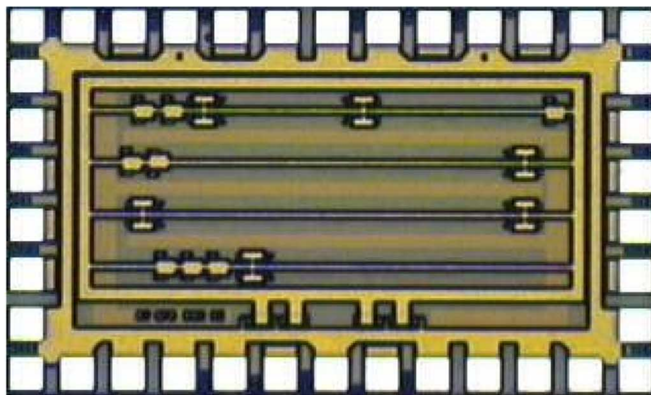
The shift registers (devices under test—DUT) were designed at Georgia Tech, and packaged at the Mayo Foundation. Two sets of heavy ion tests were performed at the Texas A &M Cyclotron Institute. In the first iteration the DUTs were subjected to Ne, Ar, and Xe ions at 15 MeV/amu. This was followed up with a second iteration where the DUTs were subjected to 15 MeV/amu Kr ion to obtain SEU response at the intermediate LET values. The angle of incidence of ion-beam was increased from normal incidence (0°) to 45° and 60° to vary the effective LET for a given ion. The DUTs, being serial shift registers, are ideal for standard Bit Error Rate Test (BERT) methods. The test set consisted of, fundamentally, a data source and an analyzer to examine the output of the DUT. The data source was a custom-built, Pseudo-Random Number (PRN) generator, which generated 2^7-1 long bit patterns. An Anritsu MP1764A, a 12.5 Gbit/s BERT analyzer, which can count bit errors and save the transmitted data stream in the vicinity of errors, was used. The data rates were continuously variable from 50 Mbit/s up to the maximum frequency of operation of a given DUT, and we typically acquired error information at several data rates of interest. A computer running Labview under Windows XP controlled the equipment, gathered the data, and provided some real-time data analysis. Further, the clock and data inputs were driven differentially with voltage swings compatible to CML voltage levels. Additional equipments such as a balun, 6 dB splitters, delay-lines, and bias-Ts were used to derive differential clock and data signals from a single RF source (Fig. 8).

V. Heavy Ion Data and Analysis

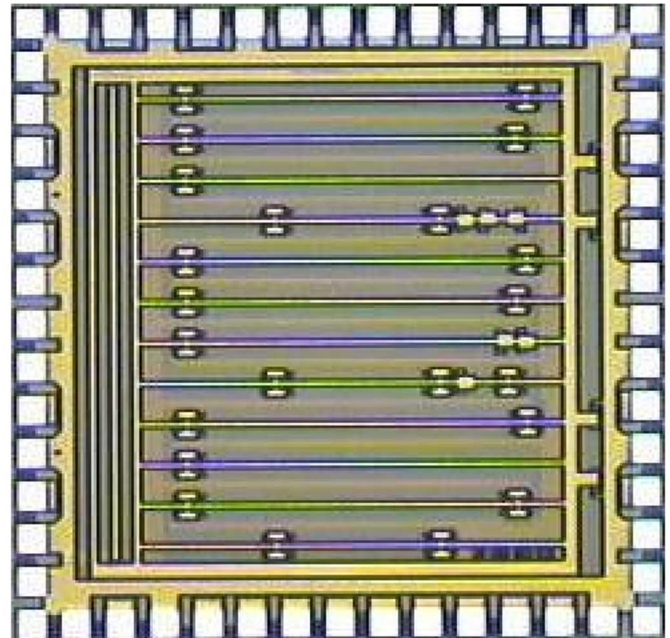
Figs. 9–11 show the heavy ion induced event cross-section (σ) as a function of effective LET for all circuits tested in this work, at various data rates. Event cross-section is chosen for representation of upsets in order to decouple the effect of varying error durations and to present only the physical ion-circuit interactions. As expected, the baseline standard MS SR displays the highest saturated device cross-section ($\sigma_{\rm sat}$) across all data rates (Figs. 9–11). The downward pointing arrows at LETs of 2.8, 5.8, and 12 MeV-cm^2/mg in Fig. 9 correspond to limiting cross-sections (i.e., no upset bits) associated with the RHBD DI TMR, GFC SR, and DI SR, respectively. Interestingly, the low-power version of the DI SR, despite having the same $I_{\rm tail}$ as the standard MS SR, but with twice as many sensitive nodes, shows $>$ 2.5× lower σ or equivalently 60% reduction in σ (Figs. 9–11) at almost all data rates. This improvement in σ is, however, higher than the estimated 1.85× improvement or equivalently 46% net reduction in σ. The 1.85× improvement in σ was estimated by combining the 73% "reduction" in transistor upset cross-section associated with using RHBD CBE SiGe HBTs in DI SR and the expected 2× degradation in σ attributable to the 2× more sensitive nodes in the DI SR compared to standard MS SR. The potential reason for higher achieved improvement could be due to the "immunity" provided by the circuit hardening technique. Note that this simplified analysis does not account for charge collection from outside the deep-trench, which was concluded to

TABLE II
COMPARISON OF POWER CONSUMPTION, AREA, AND SPEED

Topology	D-flipflop I_{tail} (mA)	Power (mW)		D-flip flop Area ($\times 10^3$ μm^2)	Max. Sim. Speed (Gbit/s)
		Total	Flipflop		
Std SR	0.5	257	11	10	6
DI SR	1.0	506	19	16	8
DI SR Low-Power	0.5	399	12	16	7
DI TMR	0.5	1136	19	16	5
GFC SR	1.0	729	40	25	8
GFC TMR	0.5	1945	33	25	5



(a)



(b)

Fig. 7. Die micrograph of a 16-bit shift register (a) and its TMR implementation (b).

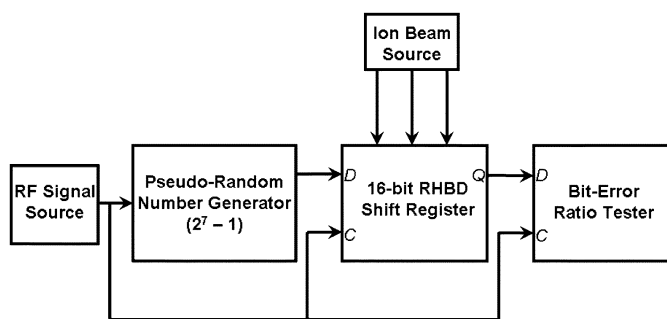


Fig. 8. Block diagram of the heavy-ion test-setup for SEU characterization of 16-bit RHBD shift registers.

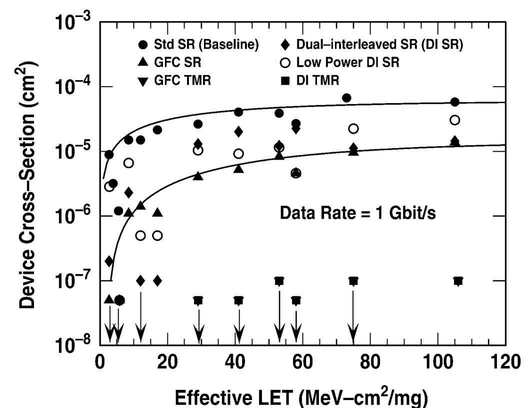


Fig. 9. Device cross-section (σ) as a function of effective LET for data rate = 1.0 Gbit/s.

be significant in second-generation SiGe HBTs [4]. This simplification further disregards the "function-related" sensitivity of individual transistors in the circuit observed in a previous work, which, however, also concluded that larger transistors present larger sensitive area [12]. The high-power version of the DI SR, as expected [14], showed significantly better performance over the low-power DI SR version at lower data rates, to a lesser extent at higher data rates, across all ion LETs. The high-power GFC SR showed the better σ_{sat} performance over DI SR at low data rates and progressively degraded as the frequency increases, but always remained better than or comparable to that of the DI SR.

The heavy ion test data showed limiting cross-sections in both "double RHBD" DI TMR and GFC TMR at 1 Gbit/s (and at higher data rates) up to an LET of 75 MeV-cm^2/mg (Fig. 9). However, at data rates below 100 Mb/s in GFC TMR and below

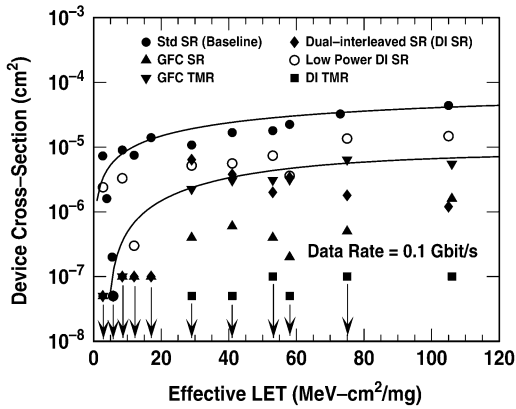


Fig. 10. Device cross-section (σ) as a function of effective LET for data rate = 0.1 Gbit/s.

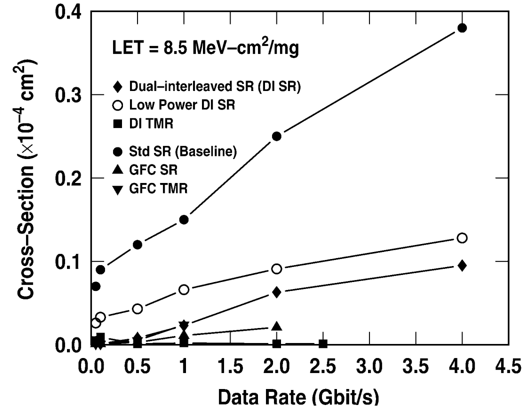


Fig. 12. Device cross-section σ as a function of data rate for $\mathrm{LET} = 8.5$ MeV-cm^2/mg.

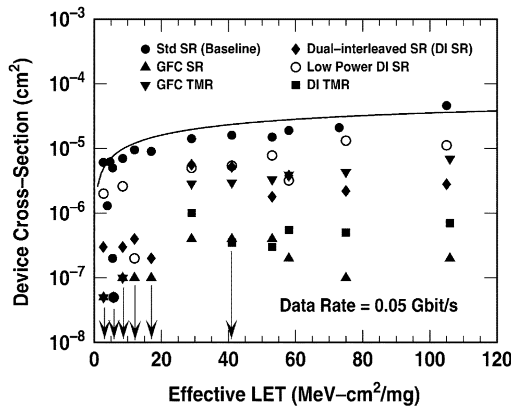


Fig. 11. Device cross-section (σ) as a function of effective LET for data rate = 0.05 Gbit/s.

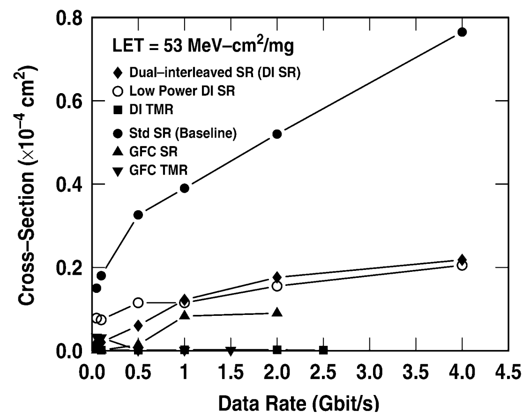


Fig. 13. Device cross-section σ as a function of data rate for $\mathrm{LET} = 53$ MeV-cm^2/mg.

50 Mb/s in DI TMR the SEU response degraded considerably. Despite this anomalous low data rate behavior, the fact that TMR offers significant improvement in the SEU response of the shift registers is in itself an important and encouraging result. Interestingly, the TMR in GFC SR did not provide as much improvement in σ at low speeds as the TMR in the DI SR (Figs. 10 and 11). In addition, the σ of GFC TMR was worse than that of high-power GFC SR at low data rates. Although this observation could possibly be explained based on the reduced bias current in the constituent shift registers, it is still puzzling to note that register-level redundancy and voting had little effect in improving the overall SEU immunity at low data rates, given that the GFC SR in itself had the best performance among non-TMR shift registers. That said, cross-section data for low-power GFC SR would be required for a more meaningful comparison.

Figs. 12 and 13 show that the event cross-section of all the shift registers except the DI TMR and GFC TMR increases with frequency at LETs values of 8.5 and 53 MeV-cm^2/mg, respectively, which is in agreement with a previous study in first-generation SiGe shift registers [2] and consistent with clock edge related SEU sensitivity. This result is evidently in disagreement with results from a previous study using second-generation SiGe technology [5], in which even though σ increased with data rate at low frequencies, a saturation of σ was noted at higher frequencies.

Figs. 14–16 capture the average error per error event as it varies with the data rate, at LETs of 8.5, 29, and 53 MeV-cm^2/mg, respectively. It is clear at LETs of 29 and 53 MeV-cm^2/mg that average errors in all of the circuits except the TMRs increases with data rate, linearly from a value of 1 at low data rates to as high as 8 at 4 Gbit/s in the unhardened standard SR. All other circuits show relatively lower average errors per event compared to the standard SR, which could possibly be due to lower upset durations in these circuits, hence resulting in lower temporal multiple bit errors. At low LETs (Fig. 14), however, average errors did not show a linear increase with data rate, except in the case of the standard SR. In fact, the average errors remained close to 1 to data rates as high as 2 Gbit/s, indicating short upset durations. Interestingly, there were no errors observed at data rates above 100 Mb/s for LETs as high as 75 MeV-cm^2/mg in the TMR shift registers and at low data rates for lower LET values in GFC SR and DI SR (Figs. 14, 15, and 16). Under such conditions average errors per event was assumed to be 0.

Table III gives a summary of our SiGe RHBD results, including threshold LETs of the various circuits. These LET thresholds were estimated in two different ways; by fitting of a standard Weibull curve to the data (L_{th}), and by using the LET value at 10% $(L_{0.1})$ of the estimated saturated cross section. For reference, at 1 Gbit/s comparison of the standard MS SR

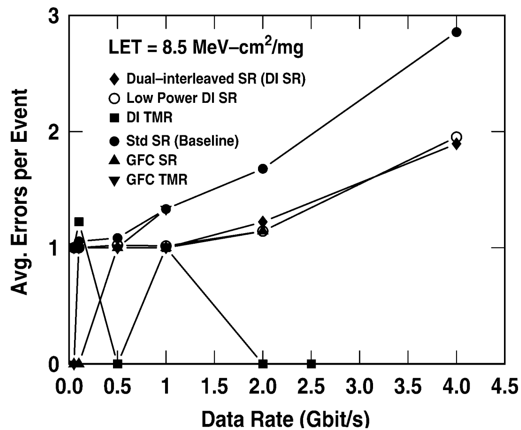


Fig. 14. Average errors per error events as a function of data rate for $\mathrm{LET} = 8.5$ MeV-cm^2/mg.

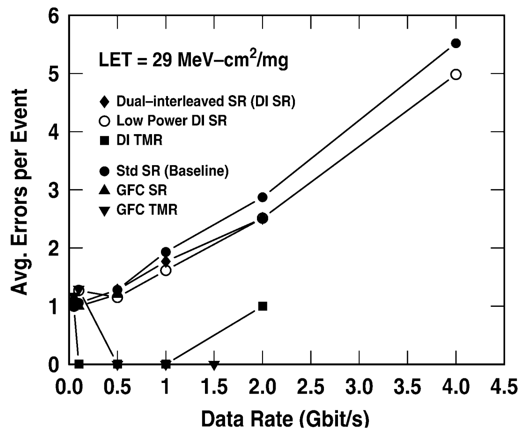


Fig. 15. Average errors per error events as a function of data rate for $\mathrm{LET} = 29$ MeV-cm^2/mg.

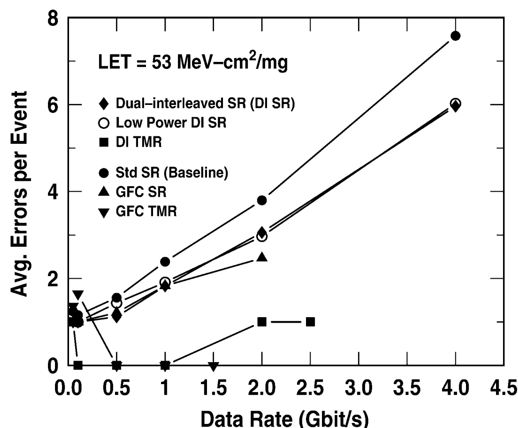


Fig. 16. Average errors per error events as a function of data rate for $\mathrm{LET} = 53$ MeV-cm^2/mg.

to the Dual-interleaved TMR SR (worst to best case), yields an improvement in threshold LET over of $7500\times$ based on Weibull fit parameter, L_{th}. This is clearly a significant improvement, and represents the first successful SEU hardening of SiGe logic circuits. We are encouraged by these results, and believe that they represent a step forward towards a potentially effective mitigation path for SEU hardening of SiGe logic using purely RHBD techniques.

TABLE III
ESTIMATED THRESHOLD LET FOR THE SHIFT REGISTERS

Topology	L_{th}		$L_{0.1}$	
	0.1 Gbit/s	1 Gbit/s	0.1 Gbit/s	1 Gbit/s
Std SR	0.01	0.01	4.0	1.8
DI SR	6.0	2.0	10.0	6.2
DI SR Low-Power	0.05	0.4	1.8	3.4
DI TMR	>75	>75	-	-
GFC SR	6.0	2.2	10.0	10.0
GFC TMR	4.0	>75	10.0	-

VI. SUMMARY

A combination of circuit- and device-level RHBD techniques was successfully applied in the realization of high-speed shift registers for the first time in IBM SiGe 8HP BiCMOS technology. The use of RHBD C-B-E SiGe HBTs with 73% smaller trench-enclosed (DT-enclosed) area than conventional C-B-E-B-C devices, and circuit RHBD techniques such as the dual-interleaving, gated-feedback, and TMR, proved effective in improving the overall SEU immunity of the shift registers, to high LET values. Limiting cross-sections were observed to a LET value of 75 MeV-cm^2/mg at 1 Gbit/s data rate in DI TMR. In addition, a significant improvement in threshold LET was observed in RHBD circuits compared to the unhardened standard CML shift register.

ACKNOWLEDGMENT

The authors are grateful to K. LaBel, L. Cohn, D. Chaney, W. Snapp, D. Radack, A. Campbell, and the SiGe team at IBM for their contributions.

REFERENCES

[1] J. D. Cressler and G. Niu, *Silicon-Germanium Heterojunction Bipolar Transistors*. Boston, MA: Artech House, 2003.

[2] P. W. Marshall, M. A. Carts, A. Campbell, D. McMorrow, S. Buchner, R. Stewart, B. Randll, B. Gilbert, and R. Reed, "Single event effects in circuit hardened SiGe HBT logic at gigabit per second data rate," *IEEE Trans. Nucl. Sci.*, vol. 47, pp. 2669–2674, Dec. 2000.

[3] D. L. Hansen, P. W. Marshall, R. Lopez-Aguado, K. Jobe, M. A. Carts, C. J. Marshall, P. Chu, and S. F. Meyer, "A study of the SEU performance of InP and SiGe shift registers," *IEEE Trans. Nucl. Sci.*, vol. 52, pp. 1140–1146, Aug. 2005.

[4] R. A. Reed, P. W. Marshall, J. C. Pickel, M. A. Carts, B. Fodness, G. Niu, K. Fritz, G. Vizkelethy, P. E. Dodd, T. Irwin, J. D. Cressler, R. Krithivasan, P. Riggs, J. Prairie, B. Randall, B. Gilbert, and K. A. LaBel, "Heavy-ion broad-beam and microprobe studies of single-event upsets in 0.20-μm SiGe heterojunction bipolar transistors and circuits," *IEEE Trans. Nucl. Sci.*, vol. 50, pp. 2184–2190, Dec. 2003.

[5] P. W. Marshall, J. C. Pickel, M. A. Carts, B. Fodness, G. Niu, K. Fritz, G. Vizkelethy, P. E. Dodd, T. Irwin, J. D. Cressler, R. Krithivasan, P. Riggs, J. Prairie, B. Randall, B. Gilbert, and K. A. LaBel, "A comparative study of heavy-ion and proton-induced bit-error sensitivity and complex burst-error mModes in commercially available high-speed SiGe BiCMOS," *IEEE Trans. Nucl. Sci.*, vol. 51, pp. 3457–3463, Dec. 2004.

[6] M. P. LaMacchia and W. O. Mathes, "SEU Hardening Approach for High Speed Logic," U.S. Patent 5 600 260, Feb. 4, 1997.

[7] B. Jagannathan, "Self-aligned SiGe NPN transistors with 285 GHz fmax and 207 GHz ft in a manufacturable technology," *IEEE Electron. Device Lett.*, vol. 23, no. 5, pp. 258–260, May 2002.

[8] S. E. Kerns and B. D. Shafer, “The design of radiation-hardened ICs for space: A compendium of approaches,” *Proc. IEEE*, vol. 76, pp. 1470–1509, Nov. 1988.
[9] D. L. Hansen, P. Chu, K. Jobe, A. L. Mc Kay, and H. P. Warren, “SEU cross sections of hardened and unhardened SiGe circuits,” *IEEE Trans. Nucl. Sci.*, to be published.
[10] R. Krithivasan, G. Niu, J. D. Cressler, S. M. Currie, K. E. Fritz, R. A. Reed, P. W. Marshall, P. A. Riggs, B. A. Randall, and B. Gilbert, “An SEU hardening approach for high-speed SiGe HBT digital logic,” *IEEE Trans. Nucl. Sci.*, vol. 50, pp. 2126–2134, Dec. 2003.
[11] G. Niu, R. Krithivasan, J. D. Cressler, P. A. Riggs, B. A. Randall, P. W. Marshall, R. A. Reed, and B. Gilbert, “A comparison of SEU tolerance in high-speed SiGe HBT digital logic designed with multiple circuit architectures,” *IEEE Trans. Nucl. Sci.*, vol. 49, pp. 3107–3114, Dec. 2002.
[12] P. Chu, D. L. Hansen, B. L. Doyle, K. Jobe, R. Lopez-Aguado, M. Shoga, and D. S. Walsh, “Ion-microbeam probe of high-speed shift registers for SEE analysis-part 1: SiGe,” *IEEE Trans. Nucl. Sci.*, vol. 53, pp. 1574–1582, Jun. 2006.
[13] G. Freeman, M. Meghelli, Y. Kwark, S. Zier, A. Rylyakov, M. A. Sorna, T. Tanji, O. M. Schreiber, K. Walter, J.-S. Rieh, B. Jagannathan, A. Joseph, and S. Subbanna, “40-Gb/s circuit built from a 120-GHz f_T SiGe technology,” *IEEE J. Solid-State Circuits*, vol. 37, pp. 1106–1114, Sep. 2002.
[14] D. R. Roth, P. J. McNulty, W. G. Abdel-Kader, L. Strauss, and E. G. Stassinopoulos, “Monitoring SEU parameters at reduced bias,” *IEEE Trans. Nucl. Sci.*, vol. 40, pp. 1721–1724, Dec. 1993.