DESIGN OF ANALOG CIRCUITS FOR EXTREME ENVIRONMENT APPLICATIONS

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DESIGN OF ANALOG CIRCUITS FOR EXTREME ENVIRONMENT APPLICATIONS

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To my parents, Soheila and Abbas,

who taught me to dream big,

and

To my soulmate, Sasan,

who has never ceased being my best friend.

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SUMMARY

Silicon-germanium (SiGe) BiCMOS technology has emerged as a compelling technology platform for implementing mixed-signal electronic circuits intended for extreme environment applications. The heterojunction bipolar transistors (HBTs) in SiGe technology offer transistor-level performance metrics comparable with those of III-V devices, while maintaining much higher levels of integration, yield, and reliability. SiGe HBTs have also additional desirable side-benefits of possessing an inherent hardness to ionizing radiation to multi-Mrad dose levels, and having immunity to enhanced low dose rate sensitivity. These unique features of SiGe HBTs make SiGe technology a strong candidate for extreme environment applications. However, it remains to be shown that the remarkable device performance of SiGe transistors translates into equally superior circuit performance under extreme environment conditions. Robust operation of analog electronics in harsh environments is a particularly challenging design problem.

This work investigates the challenges associated with designing SiGe analog and mixed-signal circuits capable of operating reliably in extreme environment conditions. Three extreme environment operational conditions, namely, operation over an extremely wide temperature range, operation at extremely low temperatures, and operation under radiation exposure, are considered. As a representative for critical analog building blocks, bandgap voltage reference (BGR) circuit is chosen. Several architectures of the BGRs are implemented in two SiGe BiCMOS technology platforms. The effects of wide-temperature operation, deep cryogenic operation, and proton and x-ray irradiation on the performance of BGRs are investigated. The impact of Ge profile shape on BGR's wide-temperature performance is also addressed. Single-event

transient response of the BGR circuit is studied through microbeam experiments. In addition, proton radiation response of high-voltage transistors, implemented in a low-voltage SiGe platform, is investigated. A platform consisting of a high-speed comparator, digital-to-analog (DAC) converter, and a high-speed flash analog-to-digital (ADC) converter is designed to facilitate the evaluation of the extreme environment capabilities of SiGe data converters. Room temperature measurement results are presented and predictions on how temperature and radiation will impact their key electrical properties are provided.

CHAPTER I

INTRODUCTION

The term extreme environment is generally used to represent the conditions outside the domain of commercial, or even military, specifications. Such environments would mandate operational conditions, for instance, outside the standard military temperature range (-55° C to 125° C), in a radiation-rich environment, in a high vibration or extremely high (or low) pressure environment, and even in a chemically corrosive environment [1]. This chapter provides an overview of the applications that mandate such extreme environment conditions for electronics and addresses the problems that conventional electronics will face when used in such harsh conditions. The advantages and disadvantages of existing practical approaches used to mitigate these problems are discussed, and finally, an outline of the thesis is given.

1.1 Extreme Environment Applications

Extreme environmental conditions are enforced for electronics in a number of important niche applications. Oil well-logging is one good example. Projections of the Department of Energy show that despite advances in alternative energy sources, petroleum will remain the major source of energy for the next 20 years [2]. However, supplies for easily recoverable oil and gas are diminishing, and the need to access the oil from wells with depths greater than 15,000 ft is rapidly rising. Exploring for oil requires probes that are sent into bore holes to monitor and steer the drill bit and send signals to the surface instrument. At depths as extreme as 15,000 ft, these signals must be sent through long cables and therefore will be subject to degradation. One solution to this problem is to have signal processing electronics co-located within the probes to multiplex signals [3]. Electronic sensors can also be used for gathering

geological information and identifying production zones. However, these electronics should survive the extreme environmental conditions that are established during the drilling process. The well temperature can vary from 150° C to 300° C, well above the military temperature range, and pressure can reach 25,000 psi. In addition, the drill is subject to high levels of shock and vibration [4].

Electronics capable of operating in extreme environmental conditions can also be used to enhance the applications for alternative energy sources such as geothermal energy. Geothermal energy is generated by the heat stored beneath the Earth's surface or by the collection of absorbed heat in the atmosphere and oceans [5]. One of the obstacles in using geothermal energy instead of natural gas to produce electricity is its associated cost, which is partly because of expensive geothermal wells. High drilling temperatures and drilling uncertainty are some of the problems that add cost to the process. To reduce the drilling time, risk, and cost, electronic circuits can be employed behind the drill bit to guide the drillers to steer the drilling process. The temperature inside these geothermal wells can rise up to 350° C, and conventional electronics would be required to be placed inside protective Dewars. These Dewars are sources of additional cost. Having electronics functioning reliably in such extreme high temperatures would eliminate the need for protective Dewars and therefore reduce the cost of geothermal energy dramatically [6].

The automotive industry can also greatly benefit from having electronics that can operate reliably at extreme environmental conditions. The government regulations with regard to mandating emission control and fuel economy have increased the need for automotive electronics, since the complex fuel control requirements could not be accomplished using traditional mechanical systems [7]. Furthermore, electronic devices are widely used in hybrid electric and future fuel cell vehicles. The underhood automotive environment, though, is a harsh environment, and automotive electronics will be exposed to extreme conditions, including high temperatures (up to 200° C

on the engine and 300° C on the cylinder, for example), wide thermal cycles, shock, vibration, fluids, and corrosive gases [4]. Conventional electronics, therefore, would require cooling and protective systems to operate reliably in an automotive environment, leading to an increase in size, weight, and cost of the product.

Another major application for extreme environment electronics is space exploration missions. Space electronics face environments with wide temperature swings, extremely low (high) temperatures, and high radiation levels, and are exposed to both cosmic rays and solar flares. During lunar exploration missions, for example, the ambient temperature on the Moon ranges from +120° C (during lunar day) to -180° C (during lunar night), with 28-day cycles. In the shadowed polar craters, the temperature could even reach as low as -230° C. More interesting places in space to explore include Mercury, where the surface temperature varies from -180° C to +425° C, Venus with a surface temperature of about +460° C, Titans with -180° C surface temperature, Mars with a surface temperature of -120° C at night, and Jupiter's Moons with a surface temperature as low as -145° C [8]. The radiation environment of space can also produce permanent and transient changes in the electrical properties of active semiconductor devices and electronic circuits. Electronics in space may be bombarded by various particles, including electrons, protons, photons, alpha particles, and heavier ions [9]. It is projected that electronics used for lunar missions can accumulate total ionization damage (TID) levels of less than 600 krad(Si) over 10 years. For Europa exploration missions, 5 Mrad(Si) of TID over 2 weeks has been reported [10]. The current approach for space missions, such as Mars rovers, is to use protective "warm boxes" and high weight shielding for radiation to provide an Earth-like environment for the electronic circuits. This technique results in excessive point-to-point wiring, increased system weight and complexity, lack of modularity, and an overall reduction in system reliability [11]. Having electronic circuits capable of functioning reliably in a space environment, without protective warm boxes, will

profoundly improve the overall space missions.

In some applications, electronics are intentionally placed in an extreme environment to improve the overall performance of a system. In radio astronomy, for example, to reduce the thermal noise of the transistors, amplifiers in the receiver are placed in a cryogenic environment [12]. The James Webb Space Telescope (JWST) project is another example. This telescope is a follow-on mission to the Hubble Space Telescope and will allow scientists to observe younger objects in space than is currently possible with the Hubble Telescope. This telescope is planned to orbit at the second Lagrange Point (L2), which is located 940,000 miles from the Earth and offers a thermally stable environment. Temperature is an essential parameter for the observation of the farthest objects. The telescope needs to be cooled to temperatures about 40 K, so it can achieve the required sensitivity in the near- to mid-infrared spectrum [13]. Therefore, electronics capable of operating robustly at such extremely low temperature will be needed.

From the above examples, one can see that, depending on the application, electronics can simultaneously be exposed to a variety of extreme environment scenarios. While the market volume for each of these applications may be small, the end-users are in fact very important, and together they form the basis for extreme environment electronics research [1]. In this work, we mainly focus on space electronics and consider three types of extreme environment conditions: 1) operation over extremely wide temperature ranges, 2) operation at extremely low temperatures, and 3) operation in radiation-intense surroundings.

1.2 Extreme Environment Issues for Electronics

There are two general approaches to obtain electronic parts required for a specific extreme environment application. The first approach is to use the existing "commercial-off-the-shelf" (COTS) products that are generally designed for multiple end-users.

These products were originally developed and specified for operation over industrial or military temperature ranges, and COTS manufacturers do not have any obligation to maintain the characteristics of their products outside their catalog-specified operating conditions. There are two ways to use COTS products for extreme environment applications. One way is to maintain these products in an environment that is within their specified operating conditions by using protective boxes. For example, for cryogenic applications, such as lunar missions, COTS products need to be kept inside warm boxes, and for high-temperature applications, such as well-logging, these products need to be placed in a Dewar to be protected from the outside extreme temperature environment. In a radiation-rich environment, strong shielding boxes will be required to protect COTS products from undesirable radiation effects. However, this technique, which is the current approach used in many extreme environment applications, increases system weight, volume, complexity, and the cost of the overall mission. Moreover, in some applications this approach becomes infeasible. For example, in a distributed control system for actuators in a rover, the electronic assemblies need to be placed on or near the motors without the option of being protected and shielded properly. Another method of using COTS products for extreme environment applications is to qualify the available parts that can actually function reliably with sufficient margin outside their catalog-specified operating conditions. In this approach, parts from different manufacturers are tested for functionality and reliability over the operating conditions mandated by the specified application. For example, the functionality of certain COTS products such as digital gate arrays and analog-to-digital converters has been demonstrated at temperatures as low as -160° C [14]. The problem with this approach is that in some cases, no commercial products are available that meet or come close to the application's requirements. In addition, once a suitable COTS has been found, if the commercial demand for that product changes or dries up, the product will no longer be available [15]. Moreover, the manufacturers

may change the fabrication process such that it still meets the commercial specifications, but the characteristics outside the catalog-specified operating conditions are significantly altered [3].

The problems associated with using COTS products for extreme environment applications have opened the path to an alternative approach, which is the development of custom-made electronics that are robust enough to withstand extreme environment conditions. The conventional hardening techniques for developing extreme environment electronics include 1) hardening-by-process (HBP), 2) hardening-by-reconfiguration (HBR), and 3) hardening-by-design (HBD) [8]. Depending on the requirements of the application, one or a combination of these three techniques is employed in implementing extreme environment circuits. Fabricating electronic devices using special materials with higher tolerance to extreme environment is one example of applying the HBP technique. Because of problems with leakage and latch-up at reverse bias junctions, conventional silicon (Si) devices fail to operate at temperatures above 200° C. Thermionic vacuum microelectronics or wide bandgap materials such as silicon carbide (SiC) support high-temperature operations up to 600° C [16]. For operations with highest temperature below 300° C, silicon-on-insulator (SOI) technology can also be an option. On the low-temperature end, because of carrier freeze out, Si-based bipolar transistors become unusable at temperatures below -130° C. The performance of Si-based CMOS transistors generally improves with cooling; however, the inferred device lifetime significantly degrades at cryogenic temperatures as a result of hot carrier degradation [17]. As is discussed in the following chapters, Silicon-Germanium (SiGe) technology is a viable technology option for low-temperature applications. For operation in a radiation-rich environment, SiGe technology offers transistors that are naturally multi-Mrad TID robust. Gallium nitride (GaN) transistors and certain classes of SiC devices are also expected to be tolerant to high doses of radiation [16]. In some cases, foundries are also willing to modify their process to

make it highly tolerant to certain extreme environment conditions such as radiation exposure. However, because of the small market for rad-hard components, the number of such foundries has decreased dramatically [18]. Overall, the HBP technique has the advantage of being an extremely reliable means of achieving hardened components. However, its disadvantages, including high manufacturing costs, low yield, and process instability, have prompted designers to adopt other hardening strategies.

HBR is another technique used for developing electronics to ensure their viability in harsh environments. In this approach, damages on electronic devices and circuits are mitigated by using re-configurable devices or adaptive self-reconfiguration of circuit topologies. For example, when device parameters are changed because of extreme environment conditions, a new circuit design, suitable for new parameter values, will be mapped into the system to recover the initial circuit functionality [8]. These new designs can be determined during or prior to the operation. Experimental results using this technique in environments with extremely high temperatures or under radiation exposure have been demonstrated in [19],[20]. One of the major risks of employing this approach is that the overhead of circuits, used to ensure reconfiguration, is also subjected to extreme environment-induced degradation. In addition, practical reconfiguration systems use switches, which can add noise and imperfections to the system [8]. Employing the HBR technique will also lead to an increase in system size and complexity.

Another promising approach to combat extreme environment-induced degradation in electronics is to apply the HBD technique. HBD can be employed at either the transistor level, by manipulating the structure of the standard transistor in a commercial foundry process, or at the circuit level, by using special design and compensation schemes. For example, using annular gate designs for nMOS transistors will help to mitigate the total ionizing radiation-induced drain-to-source leakage [21]. This leakage current leads to parametric shifts in the n-channel device and introduces

parasitics and can become crucial in radio frequency (RF) applications [22]. Several transistor-level layout-based techniques for single-event effect mitigation in SiGe HBTs, including the inclusion of an alternate reverse-biased pn junction (n-ring) to shunt electron charge away from the sub-collector [23], have also been demonstrated. On the circuit side, certain layout techniques can be employed to mitigate analog single-event transients in differential amplifiers [24]. As for wide temperature operation, standard circuit design techniques are generally not applicable [25], and new strategies need to be developed. Auto-zero correction, for example, has been used to alleviate the problem of temperature-dependent offset voltages in operational transconductance amplifiers (OTA) functioning at low temperatures [26]. The concept of HBD provides a less expensive alternative to designers compared to other techniques. Obviously, more research on applying HBD techniques for developing extreme environment circuits would be beneficial. In conjunction with HBP, HBR techniques are applied in developing analog circuits required for this work.

1.3 Thesis Outline and Contribution

The objective of this work is to investigate the feasibility of SiGe BiCMOS technology for implementing analog circuits capable of operating reliably under three extreme environment conditions: over an extremely wide temperature, at an extremely low temperature, and in a radiation-rich environment. As a representative for analog circuits, a bandgap voltage reference (BGR) circuit is considered for this study.

In Chapter 2, we study the effects of low temperature on the key device properties of CMOS transistors and SiGe HBTs. The impact of radiation on the performance of these devices is also discussed and both ionization damage as well as single-event effects are studied.

In Chapter 3, design methodologies for BGRs are discussed. Experimental results are presented, and the effects of Ge profile shape on the wide temperature performance

of these circuits are analyzed (also published in [27] and [28]).

Chapter 4 presents the measurement results for SiGe HBTs and a SiGe BiCMOS BGR circuit operating in the sub-1 K regime. Robust transistor operation of a first-generation SiGe transistor is demonstrated at package temperatures as low as 300 mK. A SiGe BiCMOS bandgap voltage reference is also verified to be fully functional at operating temperatures below 700 mK (also published in [29]). A voltage reference circuit delivaring robust performance at 37 K is designed and fully characterized.

In Chapter 5, the impact of proton irradiation on the performance of SiGe BGR circuits is presented. The circuits are irradiated at both room temperature and at 77 K. Measurement results from the experiments indicate that the proton-induced changes in the SiGe bandgap references are minor, even down to cryogenic temperatures (also published in [30]).

Chapter 6 presents a comprehensive study of the performance dependencies of irradiated SiGe precision voltage reference circuits on 1) TID, 2) circuit topology, and 3) radiation source. Two different bandgap voltage references designed in the first-generation SiGe BiCMOS technology platform are exposed to x-rays at doses of 1080 krad(SiO2) and 5400 krad(SiO2). It is shown that the degradation in circuit performance following x-ray irradiation depends on both the TID level and the chosen circuit topology. Measurement results are presented and it is concluded that large TID levels can significantly shift the magnitude of the output voltage. Explanations for the observed shifts are provided by utilizing detailed analysis of the two circuit topologies and considering device-to-circuit interactions. It is found that the primary factor responsible for the difference in the circuit response before and after irradiation can be attributed to the excess base leakage current in the SiGe HBT. To investigate the impact of radiation source, the circuit topology showing the worst-case degradation from the x-ray experiment is independently exposed to 63-MeV protons at the same effective TID level. A clear source dependence in the circuit response is observed,

and possible origins of this behavior are identified (also published in [31]).

In Chapter 7, we investigate the effects of single-event transients in the response of SiGe voltage references, voltage regulators, and data converters through ion microbeam experiments and circuit simulations. Several mitigation techniques are also discussed (also published in [32]).

Chapter 8 presents a comprehensive investigation of the impact of proton irradiation on the performance of high-voltage (HV) nMOS transistors implemented in a low-voltage (LV) SiGe BiCMOS technology. The effects of irradiation gate bias, irradiation substrate bias, and operating substrate bias on the radiation response of these transistors are examined. Experimental results show that the radiation-induced subthreshold leakage current, under different irradiation biasing conditions, remains negligible after exposure to a total dose of 600 krad(Si). It is also shown that there are differences in the radiation response of LV and HV MOSFETs, suggesting that the mechanisms involved in causing degradation in LV and HV transistors could be of fundamentally different origins (also published in [33] and [34]).

In Chapter 9, a platform for evaluating the performance of SiGe data converter under extreme environment conditions is designed and implemented in 0.12 μm SiGe technology. The platform includes a high-speed comparator, a 3-bit current steering digital-to-analog converter (DAC), and a 3-bit flash analog-to-digital (ADC)-DAC circuit. Measurement results at room temperature for both the comparator and the ADC are presented and predictions of how low temperature operation and irradiation damage will impact the performance of the comparator and the ADC are provided.

Finally, a summary of the thesis is given in Chapter 10.

CHAPTER II

EXTREME ENVIRONMENT OPERATION OF SIGE HBTS AND CMOS TRANSISTORS

SiGe BiCMOS technology offers HBTs with comparable performance to their III-V counterparts, and at the same time, maintains compatibility with conventional low cost Si CMOS foundries. As a result, SiGe BiCMOS technology has become prevalent in the domain of "mixed-signal" integrated circuits (IC), where analog, radio-frequency, and highly integrated digital circuits are all required. It has also become an appealing technology platform for building extreme environment electronics. In this chapter, we present an overview of the effects of low temperature and radiation on the key properties of SiGe HBTs and Si CMOS transistors.

2.1 Impact of Low Temperature Operation

There are many reasons that motivate the operation of electronic circuits at temperatures below the ambient temperature. Some of these reasons include: lower thermal noise and parasitic effects, improved carrier mobility, and the possibility to investigate quantum effects and physical phenomena such as single electron effects and superconductivity that only occur at low temperatures [35]. Here, we will briefly review the impacts that low temperature operation could have on the electrical properties of SiGe HBTs and MOS transistors that are important to circuit designers.

2.1.1 SiGe HBTs

Due to the presence of small amount of Ge in the base of SiGe HBTs, the device physics and operation of these transistors fundamentally differ from that of the conventional Si bipolar junction transistors. It is well known that cooling has detrimental

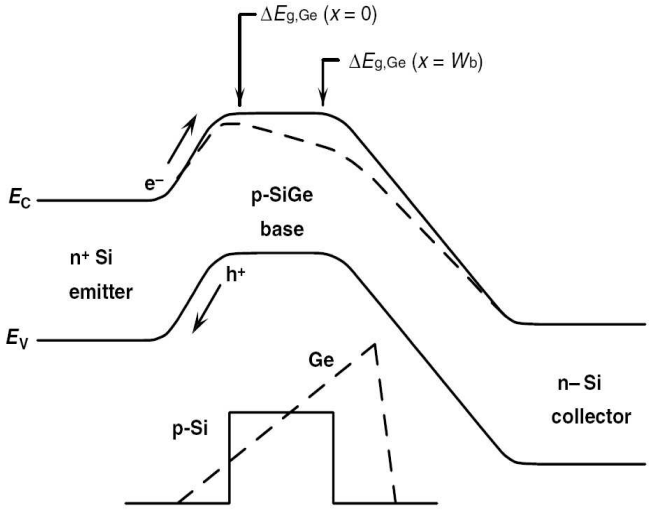

Figure 1: Energy band diagram for a Si BJT and a graded-base SiGe HBT (after [36]).

effects on the performance of Si BJTs and this precludes their application in cryogenic environments. Cooling a Si BJT will typically increase its turn-on voltage, low-injection transconductance and base resistance, will decrease its current gain and will degrade its frequency response [1]. As a result, the performance of Si BJTs strongly degrades as the temperature drops. The case is different for SiGe HBTs.

The energy band diagram for a Si BJT and graded-base SiGe HBT is shown in Figure 1 [36]. Due to bandgap engineering in SiGe HBTs, many of their key device parameters become thermally activated functions of the Ge-induced band offsets, and as a result, will improve with cooling. The presence of Ge in the base region results in two DC effects: 1) a decrease in the potential barrier to injection of electrons from emitter into the base and 2) an improvement in the output conductance of the transistor [37]. The first effect will yield higher collector current (for the same applied base-emitter voltage), and therefore higher current gain, β, compared to a Si BJT. The ratio of the current gain of a SiGe HBT, (β_{SiGe}), to the current gain of a Si BJT,(β_{Si}), can be approximated as [37]

$$\left.\frac{\beta_{SiGe}}{\beta_{Si}}\right|_{V_{BE}} \approx \frac{\widetilde{\gamma}\widetilde{\eta}\Delta E_{g,Ge}(\text{grade})/kTe^{\Delta E_{g,Ge}(0)/KT}}{1-e^{-\Delta E_{g,Ge}(\text{grade})/KT}}, \tag{1}$$

where k is the Boltzmann's constant, T is the temperature, $\widetilde{\eta}$ and $\widetilde{\gamma}$ are the minority electron diffusivity ratio and the "effective density-of-states ratio" between SiGe and Si, respectively, $\Delta E_{g,Ge}(\text{grade})$ is the Ge grading-induced bandgap offset, and $\Delta E_{g,Ge}(0)$ is the Ge-induced bandgap offset at the emitter end of the neutral base [1]. Both $\Delta E_{g,Ge}(\text{grade})$ and $\Delta E_{g,Ge}(0)$ have been denoted on Figure 9. Improvement in the output conductance (second *dc* effect) results in transistors with higher Early voltage. The Early voltage ratio of a SiGe HBT, $V_{A,SiGe}$, and a Si BJT $V_{A,Si}$ is defined as

$$\left.\frac{V_{A,SiGe}}{V_{A,Si}}\right|_{V_{BE}} \approx e^{\Delta E_{g,Ge}(\text{grade})/kT}\left[\frac{1-e^{\Delta E_{g,Ge}(\text{grade})/kT}}{\Delta E_{g,Ge}(\text{grade})/kT}\right]. \tag{2}$$

From (1) and (2), one clearly sees that the band-edge effects strongly couple into the device equations. Moreover, the band-offset parameters are divided by the thermal energy (kT). In fact, the thermal energy is arranged in these equations such that the corresponding performance metrics will improve with cooling. The dynamic response of transistors is also affected by temperature. The ratio of the base transit time of a SiGe HBT, $\tau_{b,SiGe}$ and a Si BJT, $\tau_{b,Si}$, is given by [37]

$$\frac{\tau_{b,SiGe}}{\tau_{b,Si}} = \frac{2}{\widetilde{\eta}}\frac{kT}{\Delta E_{g,Ge}(\text{grade})}\left[1-\frac{kT}{\Delta E_{g,Ge}(\text{grade})}[1-e^{\Delta E_{g,Ge}(\text{grade})/kT}]\right]. \tag{3}$$

Base transit time couples to the overall unity-gain cutoff frequency, f_T, ($f_T \propto 1/\tau_b$). As seen from (3), the Ge grading-induced base drift field aims to offset the inherent degradation in the τ_b with cooling. Hence, the frequency response will improve as the temperature drops [37]. If the base resistance, R_b does not degrade with cooling, then the maximum oscillation frequency, f_{max}, is also expected to improve at low temperatures. In fact, the base resistance in SiGe HBTs, unlike in Si BJTs, has the immunity to carrier freeze-out. This is due to the fact that highly doped thin base

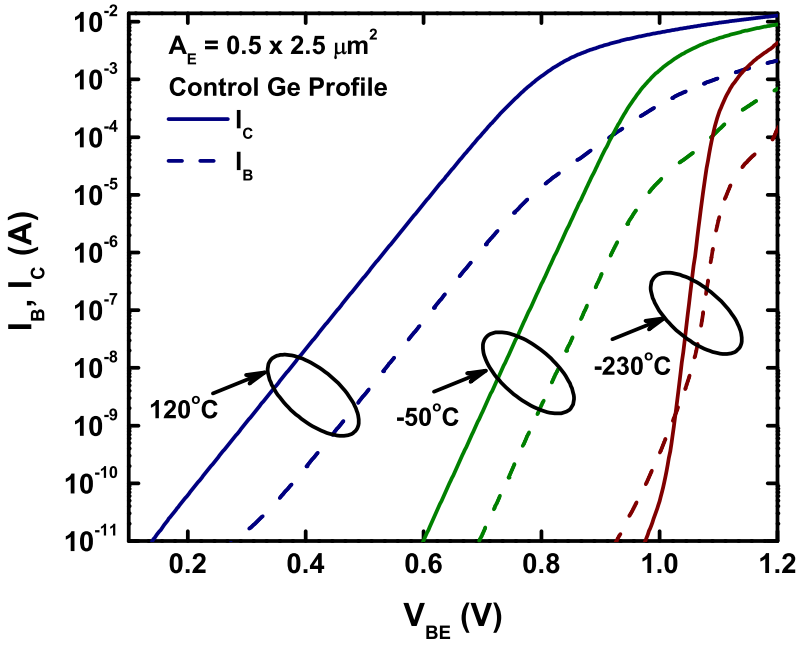

Figure 2: Forward Gummel characteristics at +120° C, -50° C, and -230° C for a SiGe HBT(after [27]).

profiles are possible by the reduced thermal cycle associated with epitaxial growth process [1].

Figure 2 shows the Gummel characteristics of a 0.5×2.5 μm^2 SiGe HBT at 120° C, -50° C, and -230° C. Due to the exponential decrease of the intrinsic carrier concentration with cooling, the base-emitter turn-on voltage increases as the temperature decreases. At -230° C, this device has a maximum current derive in excess of 4mA/μm^2.

2.1.2 CMOS Transistors

The operation of CMOS transistors at low temperatures has received considerable attention [38]-[47]. It is well known that the performance of CMOS transistors generally improves with cooling. Figure 3 shows typical subthreshold characteristics for an

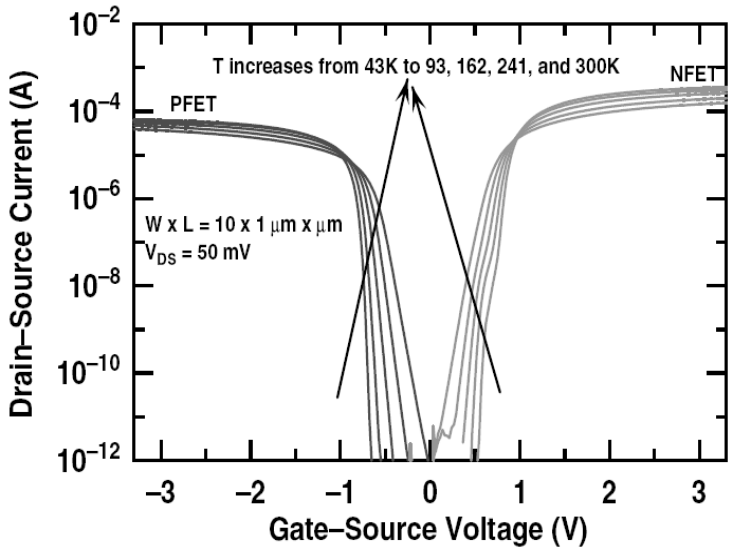

Figure 3: Subthreshold characteristics for CMOS transistors measured at different temperatures(after [38]).

NMOS and an PMOS transistor measured at 5 different temperatures, indicating that for the same bias condition, the current drive capability of the transistors increases as the temperature is reduced. Other performance improvements include a substantial increase of carrier mobility and saturation velocity, latchup immunity, lower thermal noise, lower power dissipation, better turn on voltage, and lower leakage current [40]. These enhanced transistor performances, however, come at the expense of shorter device lifetime [38]. The lifetime can be improved if transistors with longer channel lengths are used.

2.2 Cryogenic Test Facilities

- A closed-cycle helium cryogenic station made by Lakeshore Cryotronics (Figure 5) was used to characterize the circuits over a temperature range of 300 K down to 20 K. The system accepts 40-pin ceramic packages and its coaxial signal lines are suitable for measurements up to 100 MHz.

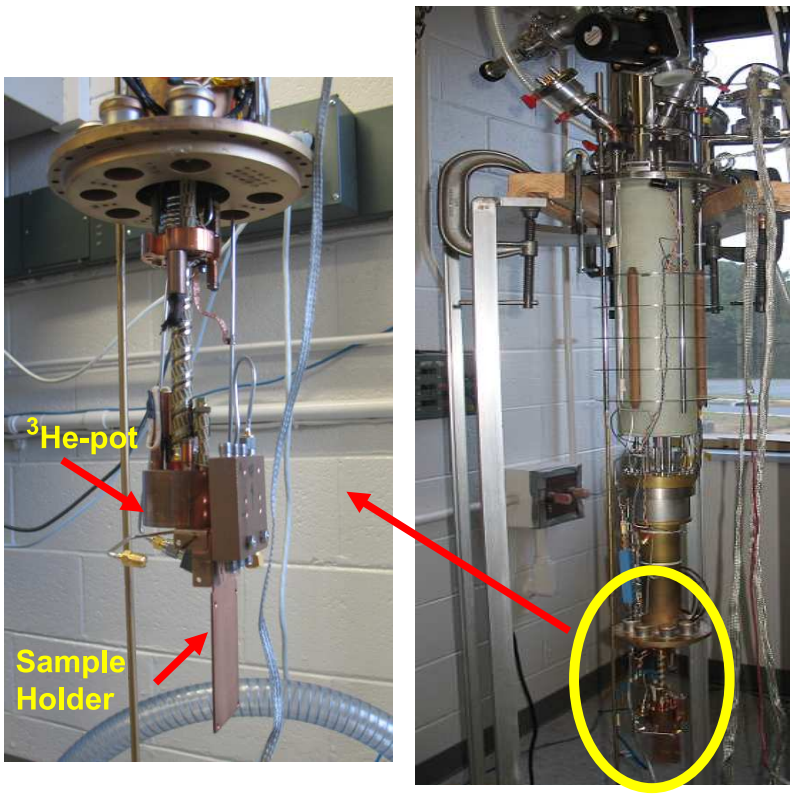

Figure 4: Photo of the heliox vertical load refrigerator, capable of reaching a base temperature of 300 mK.

- A Heliox Vertical Load (VL) refrigerator (Figure 4) at the NASA Goddard Space Flight Center was used for measurements in the deep cryogenic regime. The system is capable of reaching the base temperature of less than 300 mK with 40 μW heat load. The system reaches sub-1-K temperatures based on the reduction of entropy. The vapor pressure of a ^{3}He pot, condensed at 3.3 K, is decreased and as a result, the temperature of the system is reduced to below 1 K.

2.3 Impact of Irradiation

Due to the presence of protons and electrons trapped in the Van Allen belts, heavy ions trapped in the magnetosphere, and protons and heavy ions from solar flares, space environment is considered to be a radiation-harsh environment [48]. As a result, microelectronic devices and circuits used in space missions won't be immune from

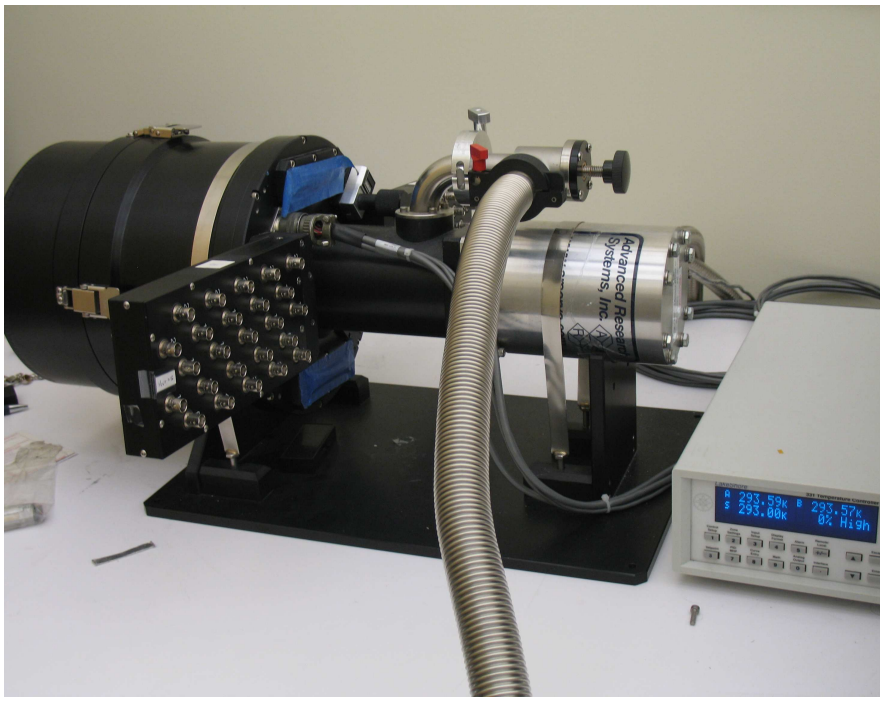

Figure 5: Photo of the closed-cycle cryogenic station.

radiation effects. Here, we will give an overview of radiation damage mechanisms in SiGe HBTs and Si CMOS transistors.

2.3.1 Radiation Damage Mechanisms

An energetic particle traversing through a solid-state material can lose its energy in several ways. The amount of energy loss depends on the projectile mass and energy, and the atomic number and mass of the target material [48]. The energy deposited per gram of material is called the dose, and is expressed in rads (acronym for radiation absorbed dose). Since this energy loss is material dependent, the type of the material is appended onto the unit, for example rad(SiO_2) indicates energy loss in SiO_2. Note that 1 rad(Si)=0.58 rad(SiO_2)=0.94 rad(GaAs). The unit "rad" can be converted to other energy density units as follows [48]

$$1 \text{ rad} = 100 \text{ erg/g} = 6.24 \times 10^{13} \text{ eV/g}. \tag{4}$$

Depending on the particle energy, device structure and material, and the irradiation source, the interaction between an energetic particle and a semiconductor transistor can damage the device in three distinct ways: 1) *ionization damage* occurs when charged particles such as protons and electrons traversing through the material, generate electron-hole pairs by disrupting the electronic bonds; 2) *displacement damage* (as the name implies) is associated with displacement of atoms from their usual lattice locations; and 3) *single event effects* occurs when the generated electron-hole pairs from the interaction between a high energy particle and the device, couple to critical circuit nodes.

2.3.2 SiGe HBTs

SiGe HBTs have a desirable side benefit of possessing an inherent hardness to ionizing radiation, and have been shown to be TID tolerant to multi-Mrad dose levels at operating temperatures as low as 77 K without any additional hardening [49]. This unique feature of SiGe HBTs is not due the presence of Ge in the base region [50] as the major source of degradation in Si transistors is the ionization damage in the emitter-base (EB) spacer oxide [48]. The radiation hardness of SiGe HBTs, is in fact a result of their inherent structural properties. Heavily doped extrinsic base region, very thin EB spacer, and very small active volume are the main technological features of SiGe HBTs that favorably help the device to be TID tolerant [1]. Yet, minor radiation-induced degradation can still be observed in the performance of SiGe HBTs. In forward-mode operation, ionization damage in SiGe HBTs will cause a slight increase in the base current at low injection (Figure 6), which will consequently degrade the current gain [49]. Although SiGe HBTs are TID tolerant, with regard to single-event effects, these devices lack immunity and require mitigation techniques that can be accomplished at the circuit level [53], or at the device level [23], or both. Figure 7 shows the transient in the collector current of a SiGe HBT that has been

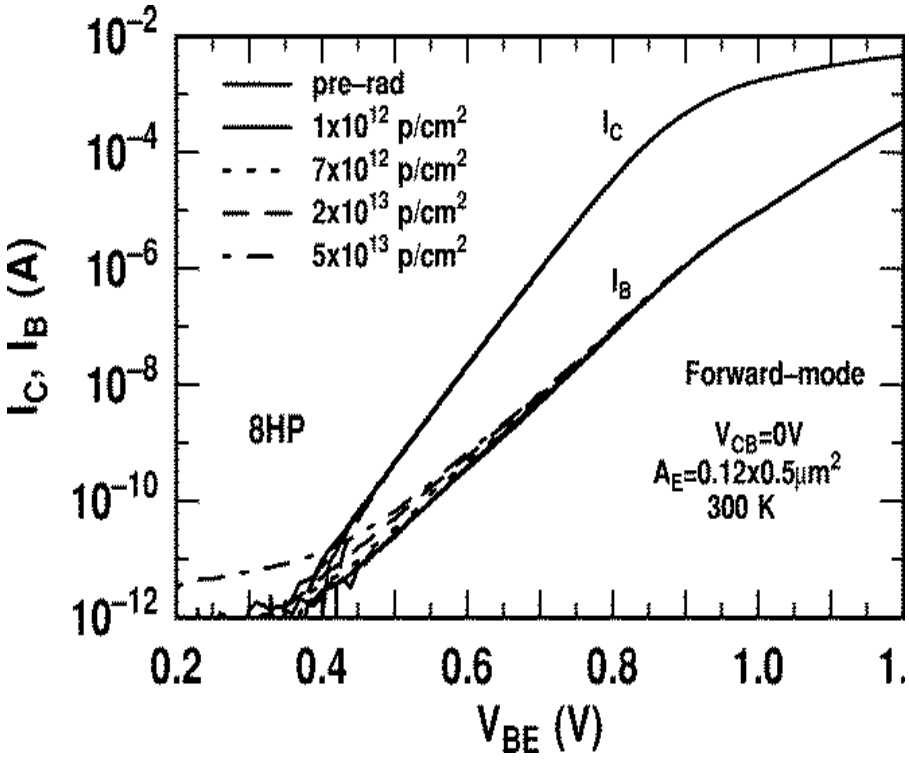

Figure 6: Forward-mode Gummel characteristics of a third-generation SiGe HBT during radiation exposure (after [51]).

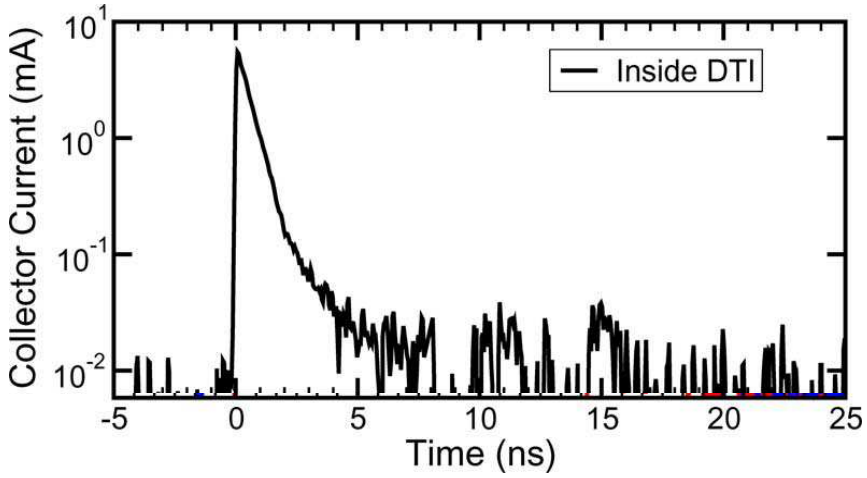

Figure 7: Collector current transients for a 5AM SiGe HBT irradiated with laser pulse (after [52]).

irradiated inside its deep trench area with laser pulse [52]. A large transient with magnitude of 1 mA and duration of 5 nS is observed. These transient spikes are able to propagate from the device through the circuit to the system, resulting in transient excursions, data corruption, and eventually system failure.

2.3.3 CMOS Transistors

In CMOS transistors, TID primarily affects the gate, spacer and field oxide layer, SiO_2. The radiation damage in the SiO_2 layer is dominated by the creation of free electron-hole pairs and their transport through the oxide [48]. A fraction of electron-hole pairs escaping the direct recombination process, will be separated by the electric filed across the field oxide. Electrons, having a much higher mobility than holes, are rapidly swept out of the dielectric, and low-mobility holes will undergo polaron hopping transport via shallow traps in the SiO_2 [54]. A fraction of these transporting holes may fall into deep traps in the oxide bulk or near the Si/SiO_2 interface forming trapped positive charge, known as oxide trapped charges. Some fraction of the holes may react with hydrogen-containing defects or dopant complexes thereby, forming the interface traps [54].

Oxide trapped charges can impact the DC response of CMOS transistors. The threshold voltage is one of the DC parameters that gets affected. If the positive oxide charge density is denoted as N_{ot}, radiation-induced voltage shift in the threshold voltage can be expressed as [54]

$$\Delta V_t = -q\frac{t_{ox}}{k_{ox}\epsilon_{ox}}\Delta N_{ot}, \tag{5}$$

where t_{ox} is the oxide thickness, k_{ox} is the dielectric constant of SiO_2, and ϵ_{ox} is the permitivity of free space. Equation (5) shows that an increase in the number of oxide-trapped charges will result in a decrease of the threshold voltage in a NMOS transistor and an increase (negatively) in the threshold voltage of a PMOS transistor. Interface traps can also impact the threshold voltage. In addition, due to

bias-dependency of trapping or detrapping of charges at the interface, the interface trap buildup increases the subthreshold swing as the device surface is swept from accumulation to inversion by the gate voltage [54]. Both interface and oxide traps will degrade the carrier mobility in the inversion layer [48]. Since defect buildup in gate oxides scales with t_{ox}, MOSFETs susceptibility to radiation-induced damage in gate oxides reduces with technology scaling [54]. Advanced CMOS technologies with smaller t_{ox}, however, require thick shallow-trench-isolation (STI) oxide (typically greater than 300 nm). As a result, spatially-distributed radiation-induced charges in the STI oxide may create parasitic inversion channels in parallel with the gate at the STI oxide edge and at the STI/body interface, resulting in an increase in the off-state leakage current [55], [56],[57]. Gate-induced leakage current (GIDL) is also increased after irradiation. Figure 8 shows the subthreshold characteristics for two nFETs from 0.42 μm (5HP) and 0.18 μm (7HP) SiGe BiCMOS technologies, prior to, and subsequent to irradiation to 100 krad. Since both technologies employ very thin gate oxide, radiation-induced shifts in the threshold voltage are negligible. Figure 8 also shows that the increase in the post-radiation off-state leakage current is significantly larger for the 5HP nFET than for the 7HP nFET. This has been attributed to STI thickness difference in the two technologies [58]. The PFETs are considered to be radiation tolerant to 1 Mrad(Si) [37].

2.4 Radiation Test Facilities

- The 76 Cyclotron of the Crocker Nuclear Laboratory at the University of California at Davis was used for proton exposure experiments. The proton energy range at this facility spans from 1.2 Mev to 68 Mev and the average particle beam flux provided, ranges from tens of particles/(cm^{2}s) up to a very large flux of approximately 10^{11} particles/(cm^{2}s) [59]. Dosimetry system uses a five-foil

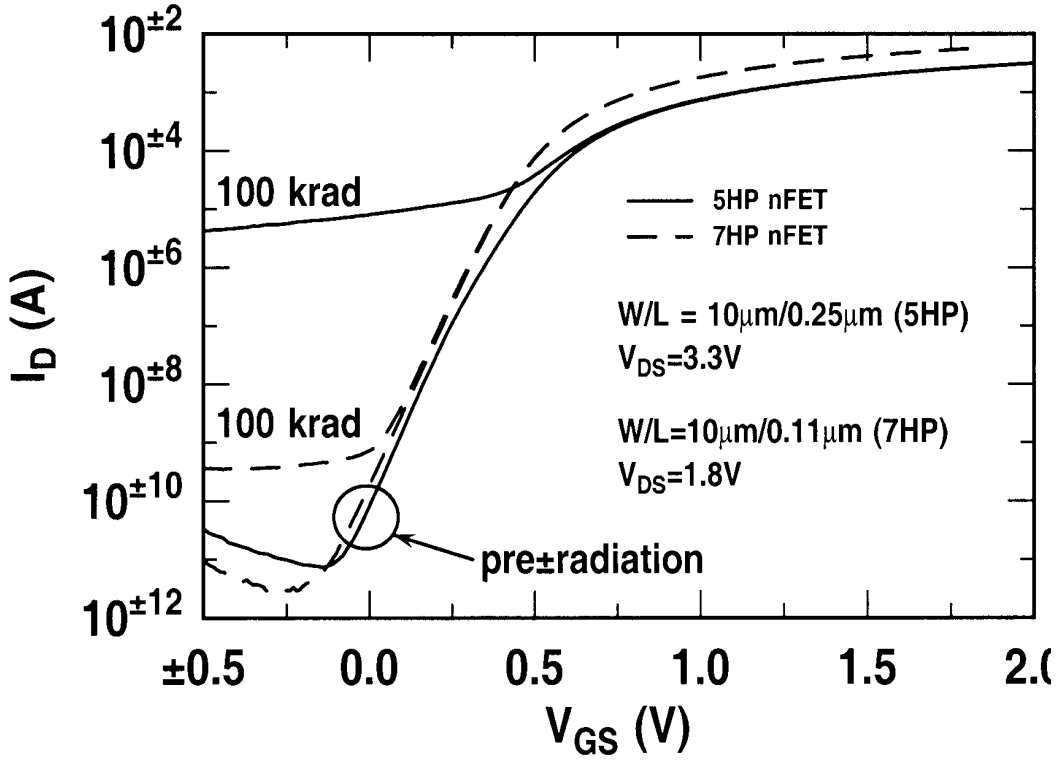

Figure 8: Subthreshold characteristics for nFETs from two SiGe BiCMOS technologies (after [37]).

secondary emission monitor calibrated against a Faraday cup, and Ta scattering foils located several meters upstream of the target establish a beam spatial uniformity of 15% over a 2.0 cm radius circular area. The dosimetry system is described in [60] and is accurate to about 10%.

- ARACOR x-ray test system at the Vanderbilt University was used for x-ray irradiation. The system produces x-rays with energies ranging from 1.00×10^4 eV to 6.00×10^4 eV and dose rates ranging from 3.33×10^{-2} rad(SiO_2)/s to 3.33×10^3 rad(SiO_2)/s.

- Time-resolved ion-beam induced charge collection (TRIBICC) testing was performed at Sandia National Laboratory using EN Tandem Van de Graaff accelerator [61], where 36 MeV ^{16}O ions were used for the heavy ion beam experiment.

2.5 SiGe Technology in This Work

For this study, two commercially available SiGe BiCMOS technologies from IBM have been utilized; first-generation 5AM and third-generation 8HP technologies. The first-generation SiGe technology (Figure 9) is a four-level metal process and features SiGe HBTs with an emitter width of 0.5 μm and a unity gain cut-off frequency (f_T) and maximum frequency of oscillation (f_{max}) of 47 GHz and 65 GHz, respectively, and nMOS and pMOS transistors with a nominal L_{eff} of 0.35 μm. The response of first-generation SiGe HBTs to proton irradiation has been reported previously [49],[50].

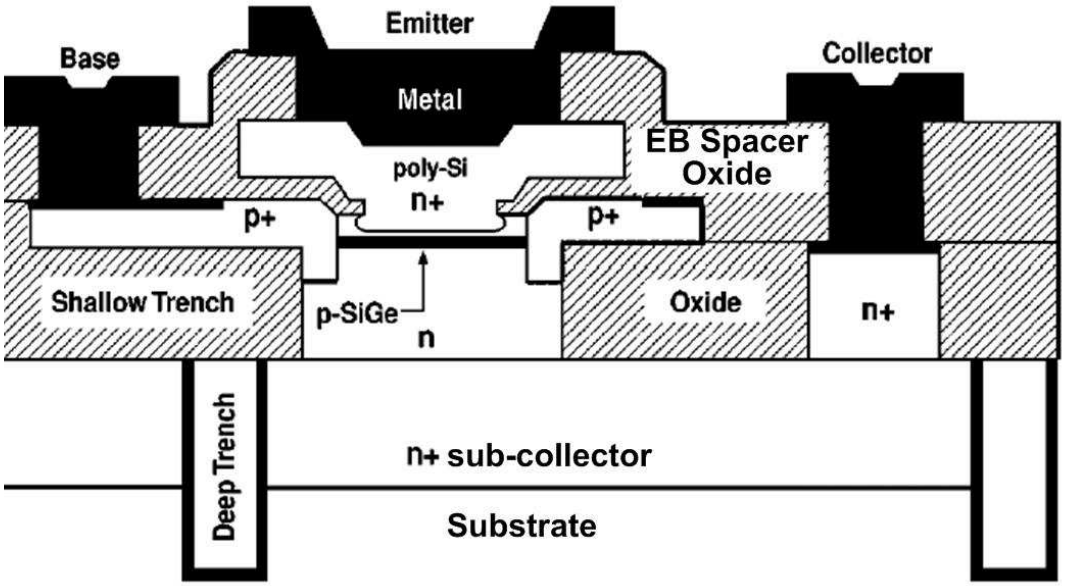

Figure 9: Cross sectional diagram of IBM 5AM technology (after [62]).

IBM's third-generation SiGe technology (Figure 10) employs a reduced thermal

Table 1: Performance metrics of IBM's first- and third-generation SiGe BiCMOS technologies.

Generation	First	Third
$W_{E,\text{eff}}$ (μm)	0.42	0.12
peak β	100	400
V_A (V)	65	> 150
peak f_T (GHz)	47	207
peak f_{max} (GHz)	65	285
BV_{CEO} (V)	3.3	1.7
BV_{CBO} (V)	10.5	5.5
L_{eff} (μm) (NMOS,PMOS)	0.35	0.092

cycle, "raised extrinsic base" structure utilizing conventional deep and shallow trench isolation, an in-situ doped polysilicon emitter, and an unconditionally stable, 25% peak Ge, C-doped, graded UHV/CVD epitaxial SiGe base [63]. The device structure has been scaled laterally to 0.12 μm emitter stripe width in order to minimize base resistance and improve the frequency response and broadband noise characteristics. Cryogenic performance and proton response of the SiGe HBTs in this technology have been previously reported in [64] and [51], respectively.

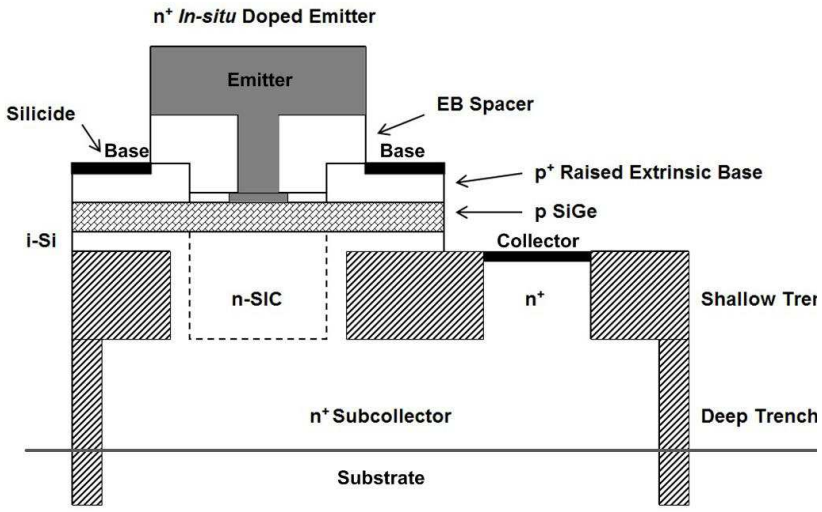

Figure 10: Cross sectional diagram of IBM 5AM technology (after [63]).

Both technologies are fully equipped with passive elements including polysilicon and diffused resistors, and various capacitors. Typical device performance metrics for these two technologies are summarized in Table 1 [37].

2.6 Summary

In this chapter, the low-temperature operations of SiGe HBTs and CMOS transistors were briefly studied. It was shown that the performances of both SiGe HBTs and CMOS transistors improve with cooling. The radiation responses of these transistors were also discussed. SiGe HBTs were shown to be TID tolerant to multi-Mrad dose levels at operating temperatures as low as 77 K. However, these devices lack immunity to single-event effects and therefore, mitigation techniques are required. For CMOS transistors, it was shown that TID increases the level of the off-state leakage current.

CHAPTER III

CRYOGENIC OPERATION OF SIGE BANDGAP VOLTAGE REFERENCES

Most, if not all, electrical circuits use a reference, be it voltage, current, or time. A reference in a circuit establishes a stable point used by other sub-circuits to generate predictable and repeatable results, and must be insensitive to variations that might occur in its operating conditions. Voltage references are extensively used in a wide variety of circuits required for extreme environment applications, including voltage regulators and high-resolution DACs and ADCs. An ideal voltage reference must be inherently well-defined and its output voltage should be independent of temperature, process, power supply, and load variations. In a data converter, for example, any change in the reference level will directly impact the converter's performance and resolution. Operation over extremely wide temperature range is a requirement for many extreme environment applications, including NASA's missions to the Moon. However, the maximum temperature range over which the performance of most of the existing electronics has been examined is the military temperature range (-55° C to +125° C).

As it was discussed in chapter 2, SiGe HBT BiCMOS technology appears to be an excellent technology platform for implementing electronics for cryogenic applications. This chapter attempts to provide answers to the questions of "will the reference circuits built in this technology show acceptable performance when operated down to deep cryogenic temperatures (e.g., -230° C)?", and "what circuit topology will give the most reliable voltage reference operation across such an extremely wide temperature range?". Several topologies of BGR circuits are implemented in two different SiGe

technology platforms. Experimental results for the wide temperature operation of the circuits are provided. The impact that the Ge profile shape could have on BGRs' wide temperature performance is also discussed.

3.1 Design of Bandgap Voltage References in SiGe Technology

A bandgap voltage references is the most commonly used topology for the implementation of a reference circuit, since its output voltage is particularly stable over temperature and process variations [65]-[81]. By definition, a bandgap reference generates an output voltage that is referred to the bandgap energy of the background semiconductor material. This bandgap energy is strongly temperature independent and its variations with temperature is negligible. For the realization of a BGR circuit at least one component with a port voltage related to the bandgap energy must be available. Since the base-emitter voltage of a bipolar transistor is related to the bandgap energy, BJTs form the core component of most bandgap reference circuits. The base-emitter voltage of a BJT can be expressed as

$$V_{BE}(T) = V_{G0} - [V_{G0} - V_{BE}(T_0)]\frac{T}{T_0} - \frac{kT}{q}(\eta - \theta)\ln(\frac{T}{T_0}). \quad (6)$$

In (6), q is the electron charge, V_{G0} is the extrapolated bandgap voltage at 0 K, $V_{BE}(T_0)$ is the base-emitter voltage at the reference temperature T_0, θ is the order of the temperature dependency of the collector current (for temperature independent collector current $\theta = 0$ and for a proportional to absolute temperature (PTAT) collector current $\theta = 1$), and η is a constant. As can be seen from (6), a complete compensation of the temperature dependency of V_{BE} with the addition of a complementary voltage, results in a voltage that is equal to V_{G0}. This is the basic idea behind the implementation of BGR circuits. Careful examination of equation (6) shows that the base-emitter voltage is actually a nonlinear function of temperature (due to the existence of the term $\ln(T/T_0)$ in (6)), and full compensation of

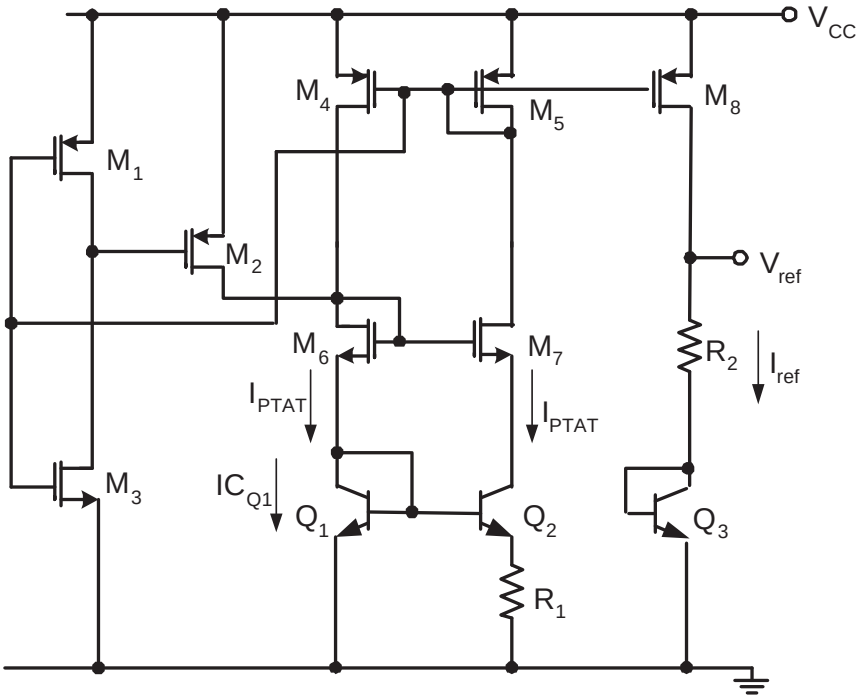

Figure 11: Schematic of the first-order voltage-mode SiGe bandgap reference.

the temperature dependency of the base-emitter voltage becomes actually a challenging problem. To address this issue, several circuit topologies have been developed; some achieve temperature compensation of the base-emitter voltage to the first degree (first-order compensation) [76], [78], [82], and some advanced architectures are able to compensate the higher-order temperature dependent terms in (6) [72], [79], [83], [74], [80]. All these reference circuits are implemented in Si technology platforms and are characterized only over either industrial or military temperature ranges.

To investigate the feasibility of SiGe BGR circuits for extreme environment applications, several different BGR circuit topologies were implemented using IBMs SiGe 5AM and 8HP BiCMOS technology platforms (Table 1). In IBM's 5AM technology, two types of first-order BGR circuits, namely, voltage-mode and current-mode, were implemented. Figure 11 shows the schematic of a first-order voltage-mode BGR in which two voltages, one proportional to the base-emitter voltage and one proportional to the thermal voltage, are summed properly to obtain a temperature-independent

reference voltage [84]. In this circuit, transistors M_1-M_3 form the start-up circuit and transistors M_4-M_7 and Q_1-Q_2, along with the resistor R_1, generate the PTAT bias current for the following stage. Each SiGe HBT used in this circuit, except for Q_2, consists of four parallel copies of 0.5×2.5 μm^2 SiGe HBTs. The emitter area of transistor Q_2 is eight times larger than that of the other transistors, and as a result, the PTAT bias current is obtained as

$$I_{PTAT} = \frac{V_{BE,1} - V_{BE,2}}{R_1} = \frac{\Delta V_{BE}}{R_1}, \tag{7}$$

where ΔV_{BE} is the difference between the base-emitter voltages of transistors Q_1 and Q_2, and is a voltage that is proportional to the absolute temperature. Transistors M_4-M_5 and M_6-M_7 are identically-sized pairs. The PTAT bias current is then amplified through transistor M_8, with the amplification factor $k = (W/L)_{M_8}/(W/L)_{M_5}$, generating I_{ref} given as

$$I_{ref} = kI_{PTAT}. \tag{8}$$

The output voltage of the first-order voltage-mode BGR, V_{ref}, can then be expressed as

$$V_{ref} = V_{BE,3} + R_2 I_{ref} = V_{BE,3} + k\frac{\Delta V_{BE}}{R_1}R_2. \tag{9}$$

The first-order negative temperature coefficient of $V_{BE,3}$ is canceled by the PTAT voltage generated across resistor R_2 and as a result, the voltage V_{ref} becomes almost equal to the bandgap voltage of SiGe extrapolated to 0 K. Note that both resistors R_1 and R_2 are implemented using the same material (here, heavily doped p-type polysilicon), and therefore, the ratio R_2/R_1 in (9) is independent of temperature and process variations. The schematic of the first-order current-mode BGR implemented in IBM's 5AM SiGe technology is shown in Figure 12. In this topology, two currents, one proportional to the base-emitter voltage and one proportional to the thermal voltage , are properly scaled and summed. The resulting current, which is going to be independent of the temperature, will then go through a resistor, generating a

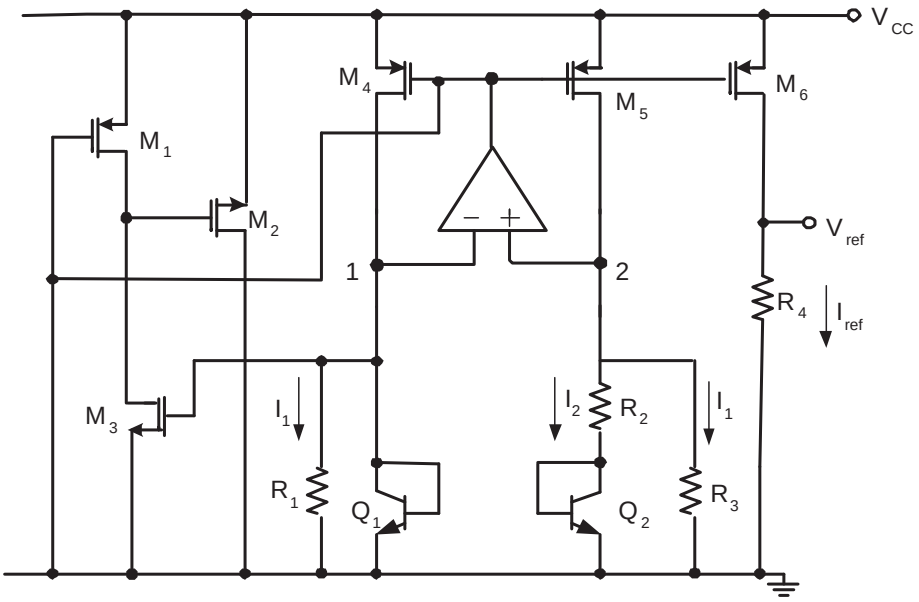

Figure 12: Schematic of the first-order current-mode SiGe bandgap reference.

temperature-independent voltage [85]. In this circuit, transistors M_1 through M_3 form the start-up circuit. The voltage across resistor R_1 is equal to the base-emitter voltage of transistor Q_1, and therefore, I_1 has a negative temperature coefficient defined as

$$I_1 = \frac{V_{BE,1}}{R_1}. \tag{10}$$

The operational amplifier drives the voltage nodes 1 and 2 to be equal to the base-emitter voltage of transistor Q_1. As a result, I_2 will be a PTAT current expressed as

$$I_2 = \frac{V_{BE,1} - V_{BE,2}}{R_2} = \frac{\Delta V_{BE}}{R_2}. \tag{11}$$

The summation of I_1 and I_2 is then flowed into resistor R_4, generating a first-order compensated output voltage defined as

$$V_{ref} = R_4(I_1 + I_2) = \frac{R_4}{R_1} V_{BE,1} + \frac{R_4}{R_2} \Delta V_{BE}. \tag{12}$$

All the resistors in this circuit are of the same type (heavily doped p-type polysilicon). Thus, the output voltage in (12) becomes insensitive to the resistors' temperature and process variations.

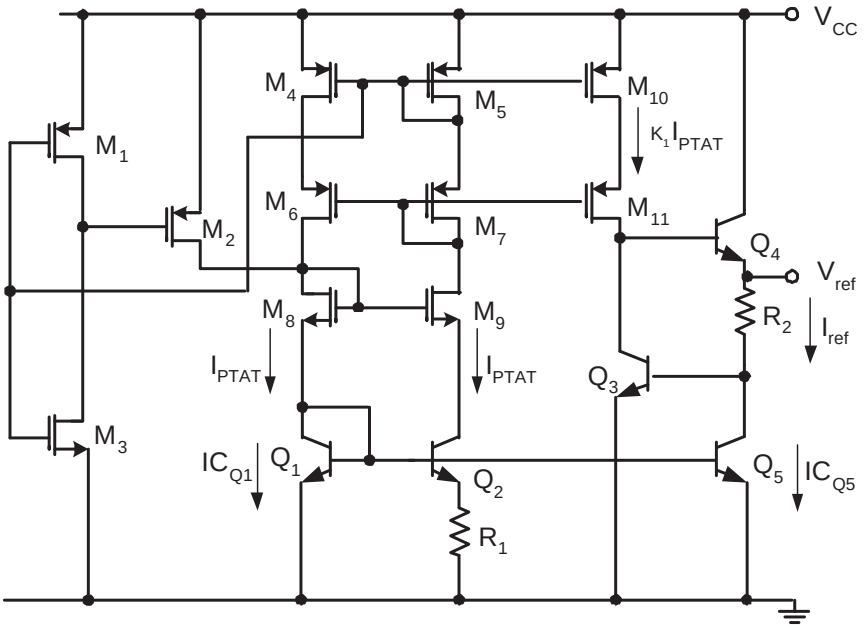

Figure 13: Schematic of the exponential curvature-compensated SiGe bandgap reference.

Since the base-emitter voltage of a SiGe HBT is a complex function of temperature, the output voltage of the first-order BGR circuit will have some inherent temperature drift. To improve the stability of the output voltage of the first-order BGR, an exponential curvature-compensation technique has been employed in another BGR circuit [83]. We refer to this circuit as the compensated BGR and its schematic is shown in Figure 13. In this circuit, the temperature characteristics of the current gain of transistor Q_3 are exploited for the curvature compensation of the output voltage. In this circuit, similar to the first-order BGR, a PTAT current is generated through transistors M_4-M_9 and Q_1-Q_2, along with resistor R_1, which follows equation (7). This PTAT current is then mirrored and amplified through the current mirrors M_{10}-M_{11} and transistor Q_5 into the following last two stages. The resulting output voltage is then estimated as [83]

$$V_{ref} \approx V_{BE,3} + R_2 I_{ref} = V_{BE,3} + k_1 \frac{\Delta V_{BE}}{R_1} R_2 + k_2 \frac{\Delta V_{BE}}{R_1 \beta_{Q,3}} R_2, \tag{13}$$

where k_1 and k_2 are the amplification factors of the PTAT current in the last two

stages, and $\beta_{Q,3}$ is the current gain of transistor Q_3. This current is almost an exponential function of temperature and therefore, the third term in (13) helps to compensate the nonlinear terms of $V_{BE,3}$. Note that because we use cascode current mirrors, the line regulation and the power supply rejection ratio of this circuit are significantly improved compared to first-order BGR circuits.

The BGR circuits implemented in IBM's 5AM SiGe technology were designed to operate with a power supply of 3.3 V. A first-order voltage-mode BGR (Figure 11) and an exponentially-compensated BGR (Figure 13) were also implemented in IBM's 8HP SiGe technology to investigate the impact of scaling on the performance of BGR circuits. These circuits operate with a power supply of 2.5 V. In all designs, careful layout techniques were employed to reduce the effects of transistor mismatch. In the following sections, we present the experimental results for the wide-temperature operation of these BGR circuits.

3.2 Operation Over Extremely Wide Temperature Range

In the context of SiGe-based BGRs, very limited studies exist [75], [77]. The work in [75] shows experimental results of a simple SiGe BGR circuit only over military temperature range. In [77], the impact of Ge grading on a simple SiGe BGR circuit over the temperature range of -55° C to 85° C is investigated using SPICE simulations.

To examine the capability of SiGe BGR circuits for extremely wide temperature range operations, and to find which circuit topology will deliver the most reliable performance in such condition, SiGe BGR circuit topologies, introduced in the previous section, were fabricated and characterized across a wide temperature range of 27°C to -230° C. For the experiments, the BGR circuits were mounted onto 28-pin ceramic DIP packages and wire-bonded. A closed-cycle helium cryostat (Figure 5) was used for DC characterization. All electrical measurements were performed using an Agilent 4155 Semiconductor Parameter Analyzer. Figures 14 and 15 show the measured

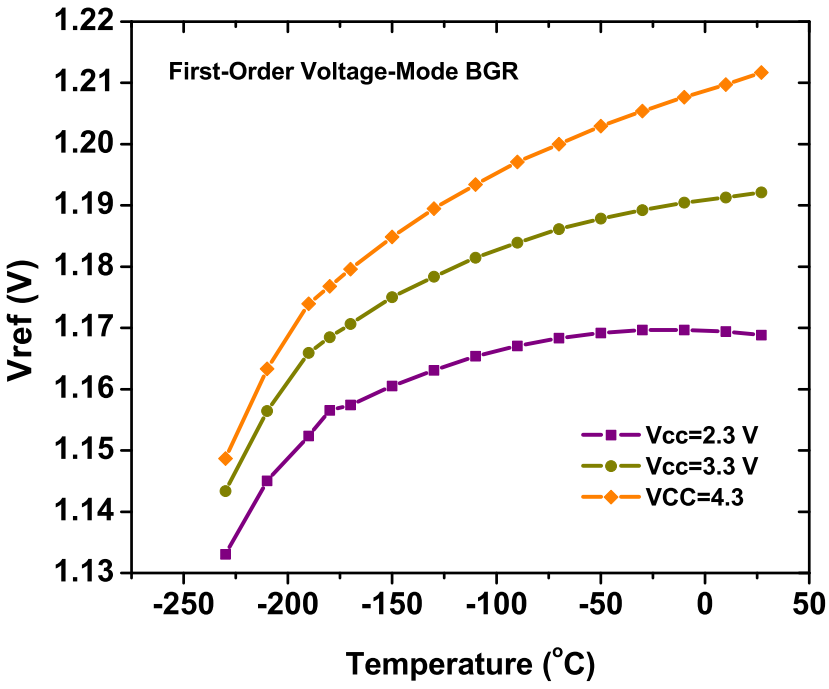

Figure 14: Measured output voltage of the first-order Voltage-Mode BGR as a function of temperature.

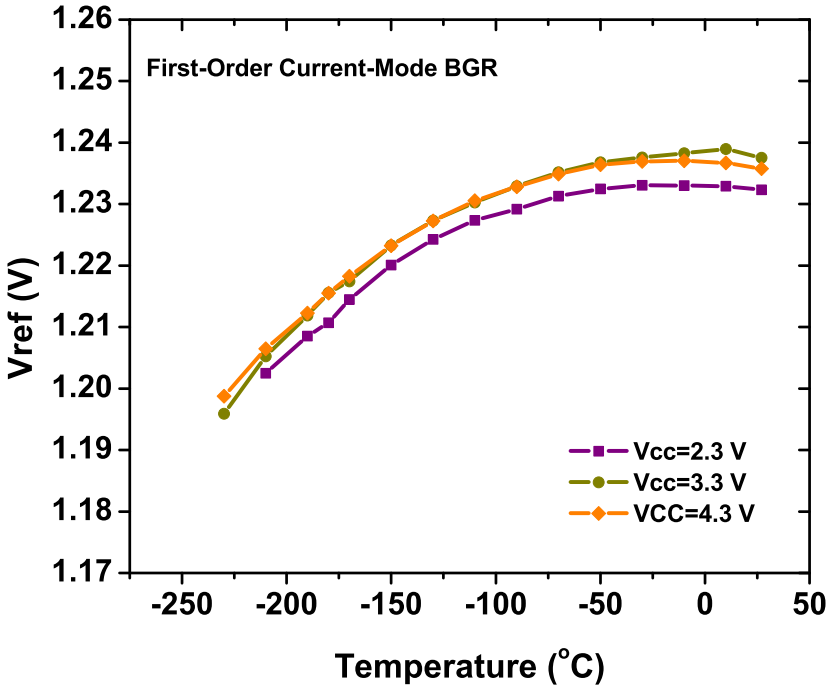

Figure 15: Measured output voltage of the first-order Current Mode BGR as a function of temperature.

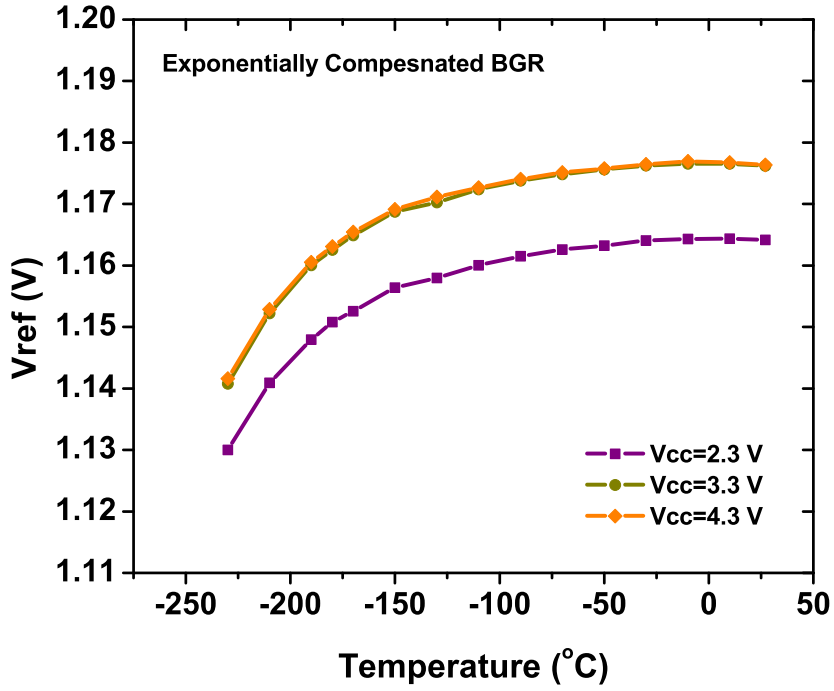

Figure 16: Measured output voltage of the exponential curvature-compensated BGR circuit as a function of temperature.

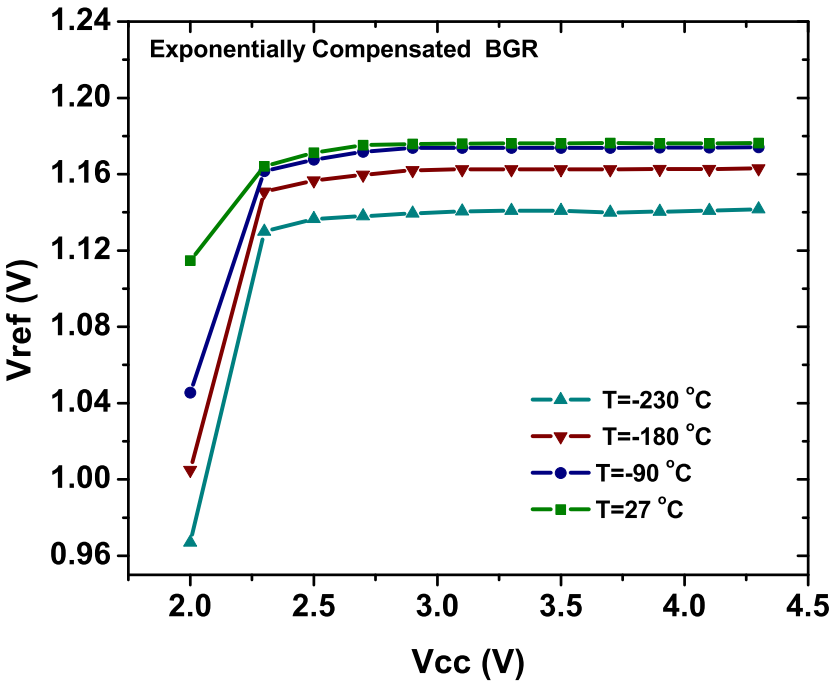

Figure 17: Measured output voltage of the exponential curvature-compensated BGR circuit as a function of power supply.

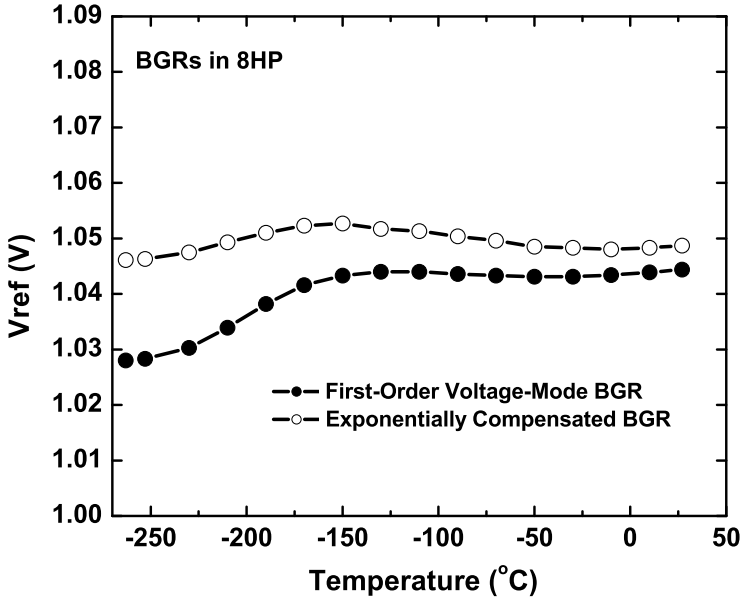

Figure 18: Measured output voltage of first-order and exponential curvature-compensated BGR circuits implemented in 8HP as a function of temperature.

output voltage of first-order SiGe BGR circuits (both voltage-mode and current-mode topologies) implemented in IBM's 5AM technology as a function of temperature for three different power supplies. Measurement results show that both circuits function well across the wide temperature range of 27° C to -230° C. The output voltage of the first-order voltage-mode circuit, however, seems to be more dependent on the power supply voltage than the output voltage of the current-mode type. This can be improved by employing cascode stages in the first-order voltage-mode circuit.

A typical metric used to evaluate the stability of a voltage reference across temperature is its temperature coefficient. This is normally expressed in parts-per-million per degree Celsius (ppm/° C) and is defined as

$$\text{Temperature Coefficient} = \frac{1}{V(T_0)} \frac{\Delta V}{\Delta T} \times 10^6, \tag{14}$$

where T_0 is the nominal temperature, $V(T_0)$ is the output voltage at the nominal

Table 2: Performance comparison of different SiGe BGR circuits

Reference	First-Order Voltage-Mode (5AM)	First-Order Current-Mode (5AM)	First-Order Voltage-Mode (8HP)	Compensated (5AM)	Compensated (8HP)
V_{ref} (V)	1.192 @ 27° C 1.168 @ -180° C 1.143 @ -230° C	1.237 @ 27° C 1.215 @ -180° C 1.196 @ -230° C	1.044 @ 27° C 1.039 @ -180° C 1.030 @ -230° C	1.176 @ 27° C 1.162 @ -180° C 1.140 @ -230° C	1.048 @ 27° C 1.050 @ -180° C 1.047 @ -230° C
TC (ppm/°C)	46.8 (-50:27) 95.9 (-180:27) 159.2 (-230:27)	22.2 (-50:27) 91.2 (-180:27) 135.4 (-230:27)	13.2 (-50:27) 23.1 (-180:27) 52.1 (-230:27)	10.6 (-50:27) 57.6 (-180:27) 118.4(-230:27)	8.4 (-50:27) 20.2 (-180:27) 17.6 (-230:27)

temperature, and ΔV is the maximum output voltage deviation across the intended temperature range ΔT. Figures 14 and 15 show that the current-mode topology has a better temperature coefficient than the voltage-mode topology. To improve the temperature stability of the reference circuit, an exponential curvature-compensated BGR was also characterized. The measurement results are shown in Figures 16 and 17. Comparing Figure 16 with Figures 14 and 15, one can see that the temperature dependency of the output voltage has significantly improved.

To evaluate the performance of SiGe BGR circuits implemented in a highly scaled SiGe technology, the first-order voltage-mode BGR and the exponential curvature-comp-

ensated BGR both designed in IBM's SiGe 8HP technology, and were characterized across temperature. In the 8HP curvature-compensated BGR circuit, the geometry of all of transistors, except for the Q_2, is $0.12\times5.0\mu m^2$. The area of transistor Q_2 consists of sixteen parallel copies of Q_1. Figure 18 shows the measurement results of the output voltage of these two circuits. As with the 5AM BGR circuits, the curvature-compensated BGR provides better temperature coefficient than the first-order BGR, as expected. Comparing Figure 18 with Figures 14 and 16 shows that BGR circuits designed in third-generation SiGe technology provide better performance and stability than the ones implemented in the first-generation technology. Table 2 provides a performance comparison for all the SiGe BGRs used in this study. A comparison of

the two exponential curvature-compensated BGR circuits implemented in IBM's 5AM and 8HP technologies with the existing state-of-the-art Si references ([72],[80]),[83]) across a more standard operating temperature range is given in Table 3.

3.3 Impact of Ge Profile Shape

The effects of Ge grading on a simple SiGe BGR circuit over the temperature range of -55° C to 85° C was first investigated using SPICE simulations in [77]. The base-emitter voltage of a SiGe HBT is expressed as [77]

$$\begin{aligned} V_{BE}(T) &= \frac{1}{q}\{E_{g0} - E_{gb}^{app} - \Delta E_{g,Ge}(0)\} - \frac{T}{qT_R}\{E_0 - E_{g0}^{app} - \Delta E_{g,Ge}(0)\} \quad (15) \\ &+ \frac{T}{T_R}V_{BE,R} + \{\frac{kT}{q}\ln\frac{I_C}{I_{C,R}} - m\frac{kT}{q}\ln\frac{T}{T_R}\} \\ &- \left\{\frac{kT}{q}\ln\left(\frac{1-\exp(-\Delta E_{g,Ge(grade)R}/kT_R)}{1-\exp(-\Delta E_{g,Ge(grade)}/kT)}\right)\right\} \\ &- \left\{\frac{kT}{q}\ln\left(\frac{T_R}{T}\frac{\Delta E_{g,Ge(grade)}}{\Delta E_{g,Ge(grade)_R}}\right)\right\}, \end{aligned}$$

where T_R, $I_{C,R}$, and $V_{BE,R}$ are the reference values of their respective parameters, E_{g0} is the Si bandgap under low doping, and E_{gb}^{app} is the bandgap energy in the presence of heavy doping. It can be seen that unlike the case with Si BJTs, the temperature dependency of the base-emitter voltage of SiGe HBTs is a complex function of temperature and the impact of Ge profile shape shows up in the equations. To further investigate the impact of Ge profile shape on the wide temperature operation of SiGe BGR circuits, two unique Ge profiles optimized specifically for cryogenic operation were developed in SiGe 5AM technology [86]. A comparison of the shape of these two Ge profiles (noted as "Cryo Ge #1" and "Cryo Ge #2") with the Ge profile in the standard 5AM process (noted as "Control Ge") is shown in Figure 19. Cryo Ge #1 and Cryo Ge #2 are the optimized cryogenic profiles designed based upon calibrated 2-D simulations over temperature, with constant stability and deeper retrograding, respectively (the latter to improve immunity to heterojunction barrier effect). Measurement results for the peak current gain and peak cutoff frequency as a function of

Table 3: Performance comparison of SiGe and Si BGR circuits.

Reference	Compensated BGR	Compensated BGR	[75]	[83]	[72]	[80]
Technology	SiGe 5AM	SiGe 8HP	SiGe 5HP	1.5 μm Si BiCMOS	6 μm CMOS	0.6 μm CMOS
V_{cc} (V)	3.3	2.5	2.5	5	-	2
V_{ref} (V) @ T = 27° C	1.172	1.026	1.328	1.264	1.192	1.142
TC (ppm/° C)	7.8 (-50:27) 28.1 (-180:27) 69.9 (-230:27)	37.3 (-50:27) 20.3 (-190:27) 27.1 (-230:27)	36.5 (-50:150) 25.1 (0:75)	3.5 (0:70) 8.9 (-55:125)	13.1 (0:70) 25.6 (-55:125)	5.3 (0:100)

temperature are shown in Figure 20. As it can be seen from Figure 20, all three Ge profiles exhibit excellent characteristics down to -230° C, while the two optimized Ge profiles give significantly better DC and AC performances at peak f_T and into high injection, as intended. More details about these two profiles can be found in [86].

An exponential curvature-compensated BGR circuit (Figure 13) was fabricated using these three Ge profile shapes for SiGe HBTs and each circuit was fully characterized over the temperature range of 27° C down to -230° C. The deviation from base-emitter voltage linearity, $\Delta_{linearity}$, is defined as

$$\Delta_{linearity} = V_{BE}(T) - (V_{BE}(T_L) - \frac{V_{BE}(T_L) - V_{BE}(T_H)}{T_L - T_H}(T_L - T)), \qquad (16)$$

and is plotted for transistor Q_3 in Figure 22 for the temperature range of T_L=-180° C to T_H=27° C.

Note that transistor Q_3 is biased with a PTAT current. The metric $\Delta_{linearity}$ has usually been reported for the case when the transistor is biased at fixed collector current [77]. However, in many BGR topologies, the collector current for the transistors inside the circuit is instead the PTAT current. Calibrated 2-D simulations of $\Delta_{linearity}$ for a single transistor with a size of Q_3, at fixed biased current and comparable collector-base voltage, are different from the measured results at the PTAT current for each of the three Ge profiles. Measurement results show that the Cryo Ge

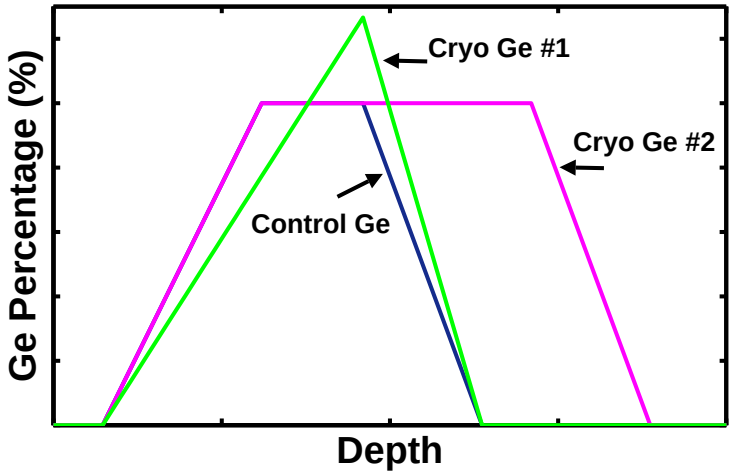

Figure 19: Ge profile shapes.

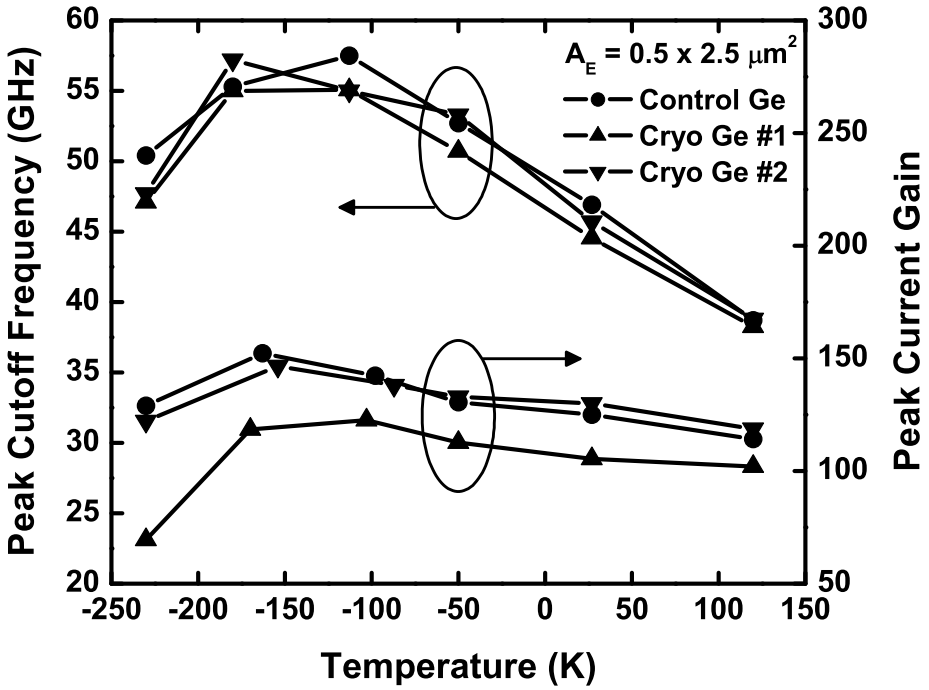

Figure 20: Measured results for the maximum current gain and peak f_T as a function of temperature for three Ge profiles.

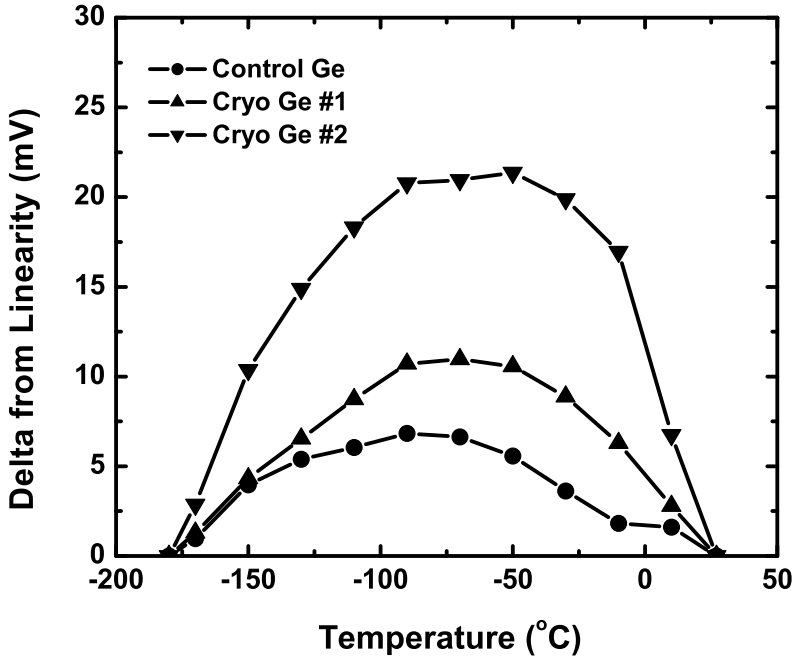

Figure 21: Measured deviation from linearity for a SiGe HBT biased with a PTAT current for the three Ge profiles.

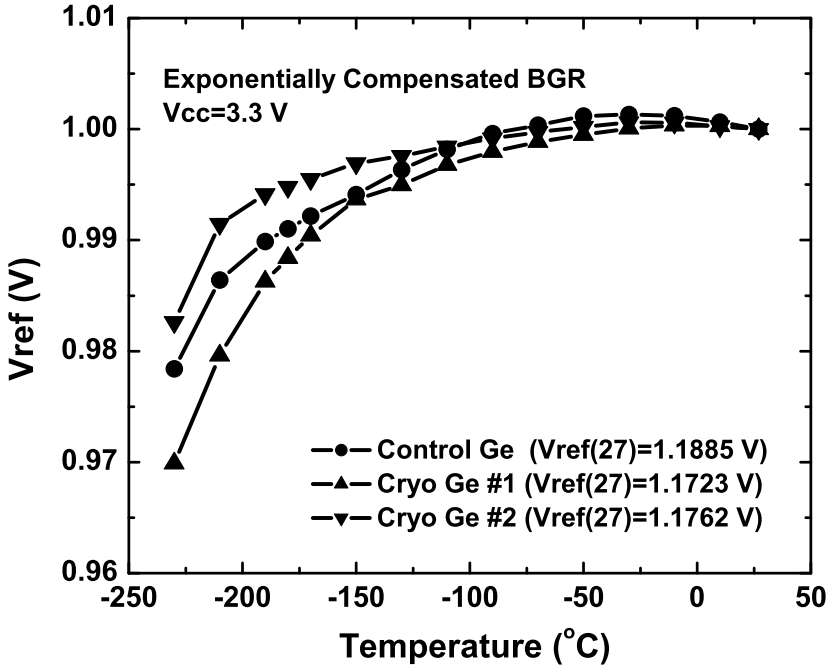

Figure 22: Measured output voltage of exponential curvature-compensated BGR circuit as a function of temperature for three Ge profiles.

Table 4: Performance metrics for exponential curvature-compensated BGR circuit implemented in three different SiGe profiles

Ge Profile	Control Ge		Cryo Ge #1		Cryo Ge #2	
V_{ref} (V)	1.1885	(27° C)	1.1723	(27° C)	1.1762	(27° C)
@	1.1778	(-180° C)	1.1662	(-180° C)	1.1625	(-180° C)
V_{cc} = 3.3 V	1.1629	(-230° C)	1.1519	(-230° C)	1.1408	(-230° C)
I_{cc} (μA)	139	(27° C)	126	(27° C)	130	(27° C)
TC (ppm/° C)	17.1	(-50:27)° C	10.6	(-50:27)° C	7.8	(-50:27)° C
@	49.8	(-180:27)° C	57.6	(-180:27)° C	28.1	(-180:27)° C
V_{cc} = 3.3 V	89.1	(-230:27)° C	118.4	(-230:27)° C	69.9	(-230:27)° C

#2 has the maximum deviation from linearity, while the Control Ge profile results in the minimum deviation from linearity over temperature. The output voltage of the reference circuit as a function of temperature for the three Ge profiles is shown in Figure 22. For ease of comparison, the output voltage for the circuit in each profile was normalized by dividing it to its nominal voltage at 27° C. It can be seen that circuits with Cryo Ge #2 and Cryo Ge #1 profiles show the best and the worst temperature coefficients among the three profiles, respectively. The temperature coefficients for the three profiles are summarized in Table 4. Our best case result of 28.1 ppm/° C for the cryo Ge profile #2 from 27° C to -180° C, more than satisfies the required specifications for many cryogenic applications.

3.4 Summary

We presented measurement results of the bandgap voltage references implemented in two different IBM BiCMOS SiGe technologies. Different architectures for the BGR were explored. All circuits operate reliably over an extremely wide temperature range. Bandgap voltage references designed in the highly scaled 8HP technology platform showed to be more robust with respect to temperature variation. The impact of Ge profile shape on the performance of BGR circuits was also investigated.

CHAPTER IV

OPERATION OF SIGE DEVICES AND CIRCUITS AT EXTREMELY LOW TEMPERATURES

Sub-millimeter wave-length astronomical instrumentation generally requires readout circuits and detectors which can reliably operate in the deep cryogenic temperature regime, so that thermal noise is strongly suppressed and the overall performance of the system is improved. Analog circuits such as voltage and current references, as well as amplifiers, are essential components of such detectors and readout circuits [87]-[90]. As discussed earlier, due to severe limitations in functionality of conventional semiconductor devices at extremely low temperatures, these requisite electronic circuits are required to be operated at temperatures considerably higher than the detectors operating temperature. A schematic diagram of a detector readout circuit used in x-ray spectrometer is shown in Figure 23 as an example [91]. The JFET gives reliable performance at a significantly higher temperature than the detector's. Therefore, the system consists of several cryogenic coolers (one for the electronic circuits and others for the remaining detector components) so that multiple temperatures can be provided [88], [90], [91]. If the electronic circuits could be designed to operate at the detectors operating temperature, the need for large numbers of signal wires providing connections between intermediate cryogenic coolers would be eliminated, resulting in dramatic reductions in system weight and volume, and the cost of the overall mission.

In this chapter, we will investigate the capability of SiGe transistors and circuits for operation at deep cryogenic temperatures. Sub-1-K functionalities of SiGe HBTs and a SiGe BGR circuit are demonstrated. In addition, a voltage reference circuit delivering robust performance at 37 K is successfully realized and characterized at 37

K.

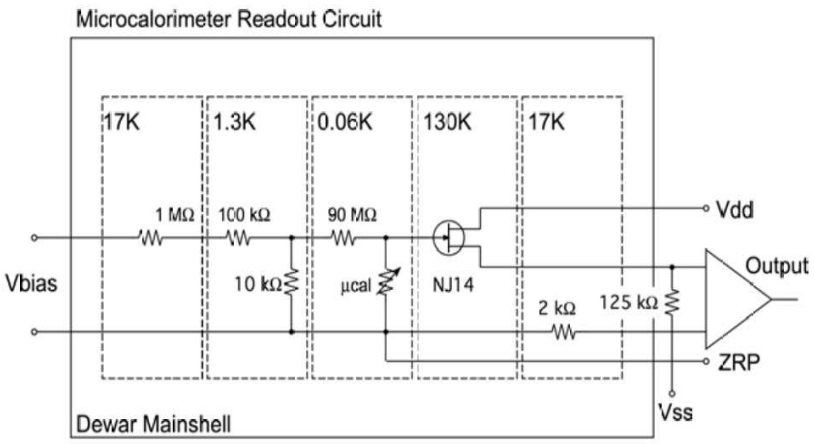

Figure 23: schematic diagram of a detector readout circuit used in x-ray spectrometer (after [91]).

4.1 Sub-1-K Operation

As it was discussed in the previous chapters, SiGe BiCMOS technology has emerged as a compelling technology platform for implementing electronic circuits intended for extreme environment applications. A substantial amount of the available information on the cryogenic operation of SiGe HBTs and circuits has been limited to a lower temperature bound of about 4.2 K (liquid-helium temperature) [92]-[97] and no data is available on the capability of SiGe HBTs and circuits for operation below 4.2 K. Since many transistor-relevant parameters (e.g., carrier density) are thermally-activated (proportional to $\exp(E/kT)$), the impact of temperature on the carrier distributions between say 4.2 K and 300 mK, is enormous (e.g., if E = 1 eV, a change by a factor of $\exp(17,943)$ theoretically exists in intrinsic carrier concentration between 4.2 K and 300 mK). As a result, it is widely believed that Si bipolar transistors will not function at sub-1-K temperatures. Note that carrier freeze-out is minimized in SiGe

HBTs, since the base, emitter, and significant portions of the collector are doped well above 3×10^{18} cm^{-3}, a minimum required doping level in Si for the occurrence of the semiconductor-metal (Mott) transition [1], [37], [98]. In this section we present the first DC measurement results for SiGe HBTs operating in environments as low as 300 mK. In addition, the operation of a SiGe BGR is fully verified for operation in the sub-1-K regime.

4.1.1 Experimental Setup

An exponential curvature-compensated BGR circuit (Figure 13) implemented in IBM's 5AM technology was selected for this study. HBTs with an emitter area of $4\times0.5\times2.5$ μm^2 were chosen as device structures. The transistors along with the SiGe BGR were mounted into a 48 pin ceramic flat-package and wirebonded. The package was epoxied into a copper sample holder and was mounted on the copper cold stage of a pumped ^{3}He refrigerator capable of reaching a base temperature of less than 300 mK under a 40 μW heat load (Figure 4). A calibrated ruthenium-oxide temperature sensor was located nearby to obtain the temperature of the cold stage. In addition, a Cernox temperature sensor, CX-1010-BR [99], was mounted adjacent to the die in the package, to closely monitor the dies temperature during the experiment. This temperature sensor is a sputter-deposited thin film resistor with a negative temperature coefficient. The measured resistance of the Cernox as a function of the ^{3}He pot temperature, at 252 mK, and for a temperature range of 400 mK to 800 mK, is shown in Figure 24. A photomicrograph showing the location of the sensor and die in the package is shown in the inset of Figure 24. It can be seen that a sensor resistance value of 600 Ω or larger corresponds to die temperatures lower than 800 mK. Transistor DC characterization was performed using an Agilent 4155 Semiconductor Parameter Analyzer. The output voltage of the BGR circuit was recorded as a function of temperature, during both cool-down and warm-up, using precision Agilent meters.

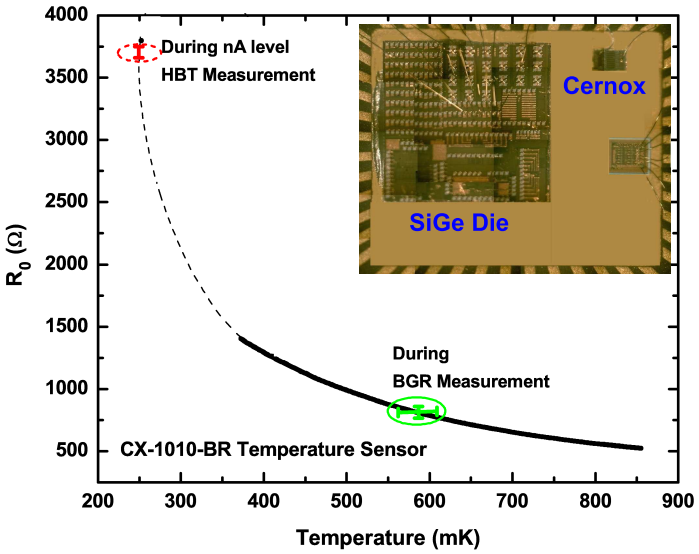

Figure 24: Measured characteristics of the on-package Cernox resistor as a function of the measured ^{3}He-pot temperature.

4.1.2 Experimental Results

The refrigerator reached a base temperature of 252 mK with no extra heat load injected into the system. The system was maintained in this state for 50 minutes prior to performing DC characterization to ensure equilibration. In order to verify the functionality of SiGe HBTs at this base temperature, forced-IB output characteristics were measured at nA-level currents to establish transistor action. During these measurements the total power injected into the system was kept below 40 μW. Shown in Figure 25, are the output characteristics of the SiGe HBT taken at 4.0 K, 1.4 K, and 252 mK, for base currents of 40 nA to 100 nA. The characteristic of the Cernox resistor during these measurements is shown in Figure 26 which shows that the package temperature remained below 300 mK (Figure 24). As it can be seen, clear transistor functionality is observed, and at the base current of 100 nA, a maximum current gain of 9.2 is achieved at package temperatures lower than 300 mK. At a

VCE of 1.0 V, and IB of 100 nA, the power dissipated by the SiGe HBT is estimated to be around 1 μW at this temperature. Forced-IB output characteristics at higher base current levels, as well as the full Gummel characteristics, were also measured and the transistor showed reasonably ideal behavior. However, due to the injection of relatively large amounts of heat during these measurements, a temperature rise was observed in the package.

Figure 27 shows the measured output voltage of the SiGe BGR circuit operating over a 1,200-second window at a sub-1-K operating temperature. The measured resistance of the Cernox sensor during this measurement is shown in Figure 28. The average output voltage obtained during this period was 1.1562 V, and the voltage deviation from the average value was less than 800 μV. With a 3.3 V power supply, the circuit consumes an average current of 39.5 μA and dissipates 130 μW. During the measurements, the package temperature stayed below 700 mK (Figure 24). The observed fluctuations in the output voltage can be further decreased by adding an on-chip capacitor at the output node.

The measured output voltage as a function of package temperature is shown in Figure 29. As explained in chapter 3, the output voltage of the BGR circuit (Figure 13) can be estimated as

$$\mathrm{V}_{out}=\mathrm{V}_{BE,3}+\frac{\Delta V_{BE}}{R_1}(k_1R_2+\frac{k_2R_2}{\beta_{Q,3}}), \quad (17)$$

where k_1 and k_2 are the amplification factors of the PTAT current in the last two stages. We point out that the circuit was originally designed and optimized for the military specification temperature range (-55° C to +125° C). One can see from Figure 29 that as the temperature drops below 220 K, the rate of increase in the base-emitter voltage is dominated by the rate of decrease in the PTAT voltage, and as a result, the output voltage decreases as the temperature is reduced. Below 36

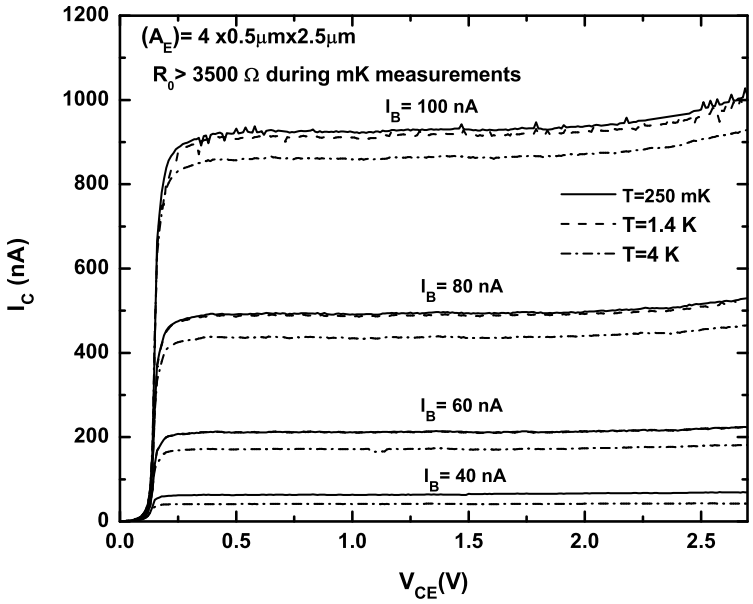

Figure 25: Measured forced-IB output characteristics of a $4\times0.5\times2.5$ μm^2 SiGe HBT at 4 K, 1.4 K, and below 300 mK.

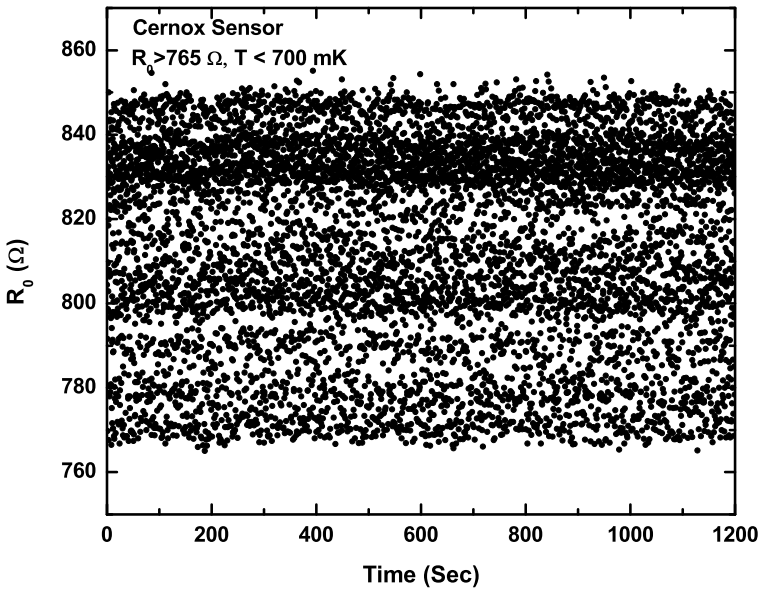

Figure 26: Measured resistance of the Cernox sensor during HBT measurements.

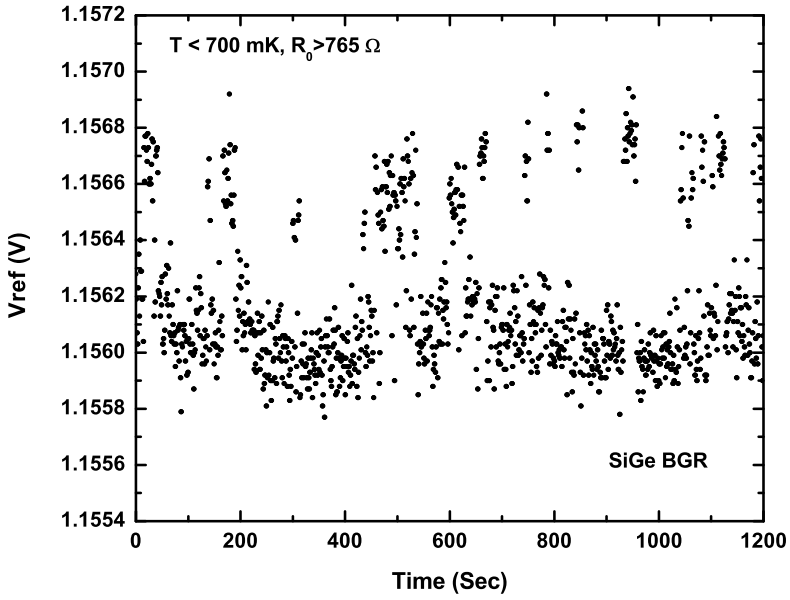

Figure 27: Measured output voltage of a SiGe BGR over 1,200-s window when operating at temperatures below 700 mK.

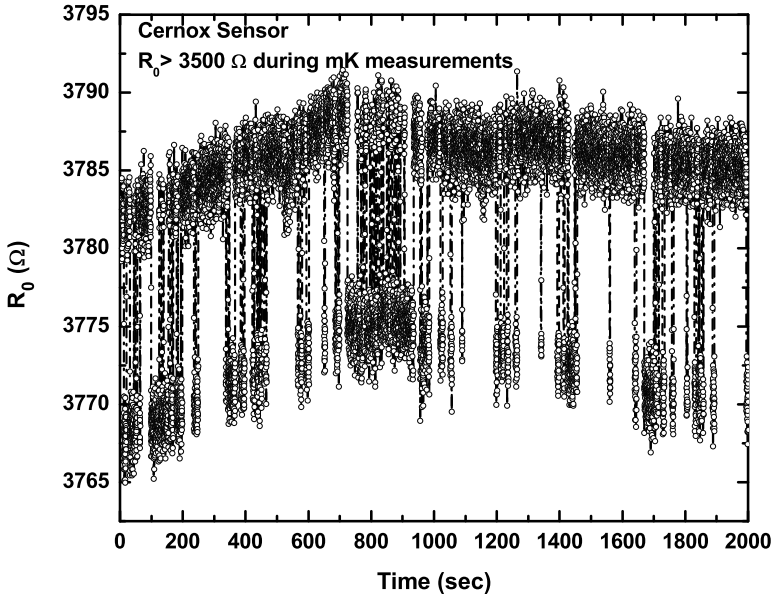

Figure 28: Measured resistance of the Cernox sensor during BGR measurements.

K, however, the output voltage begins to rise. This is due to the fact that the non-linearity in the temperature variation of the base-emitter voltage becomes more severe at these extremely low temperatures [100] and its first-order temperature coefficient is therefore decreased. As a result, the ΔV_{BE} voltage (second term in (17)) will no longer vary linearly with temperature, and instead it becomes a weak function of temperature. Therefore, the output voltage starts to increase, as the negative temperature coefficients of $V_{BE,3}$ becomes the dominant factor. Although we expect this trend to continue down to mK temperatures, a slight decrease in the output voltage is observed when the temperature is further decreased below about 4K. More investigation is required to understand this behavior. Figure 29 verifies that the exponential curvature-compensated SiGe BGR circuit is fully functional across the temperature range of 700 mK to 300 K, with a temperature coefficient of 160 ppm/° C.

4.2 Operation at 37 K

Another example of applications that requires electronics to be exposed to an extreme environment condition is the James Webb Space Telescope project. This telescope needs to be cooled to temperatures in the vicinity of 40 K so it can achieve the required sensitivity in the near- to mid-infrared spectrum [13]. As a result, electronics capable of operating robustly at such ultra low temperatures will be needed. One of the system requirements calls for the design of a voltage reference mounted on the ASIC package that can robustly generate an output voltage of 1.2 V with a power supply of 3.3 V, at operating temperature of 37 K. To investigate the feasibility of SiGe technology for this application, SiGe BGR circuits were developed using IBM's 5AM SiGe BiCMOS technology. Based on the measurement results of different BGR circuit topologies, an exponential curvature-compensated BGR circuit was selected as the core of the voltage reference. To make sure the circuit will generate an output

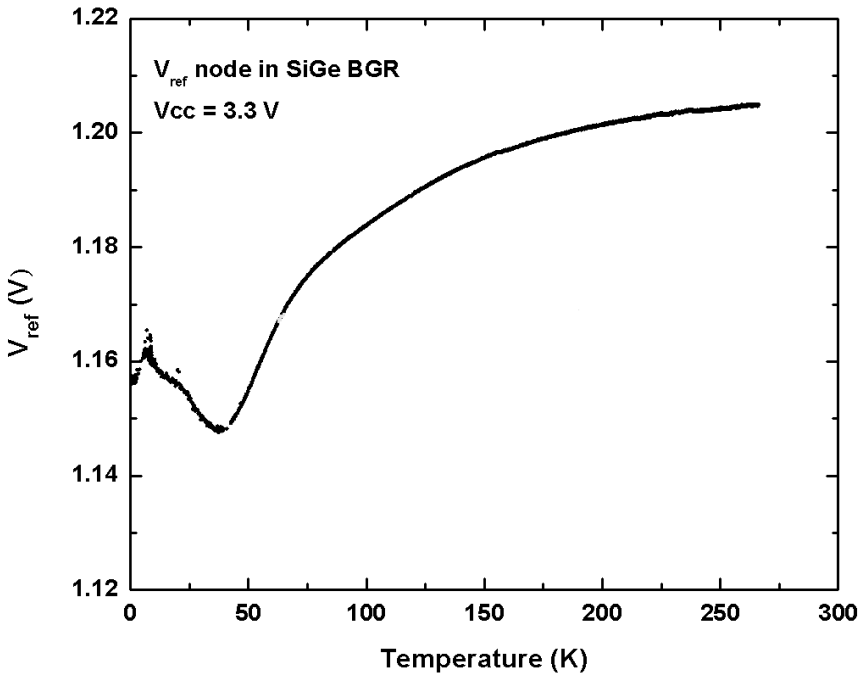

Figure 29: Measured output voltage (1,526,900 points) of the SiGe BGR as a function of temperature.

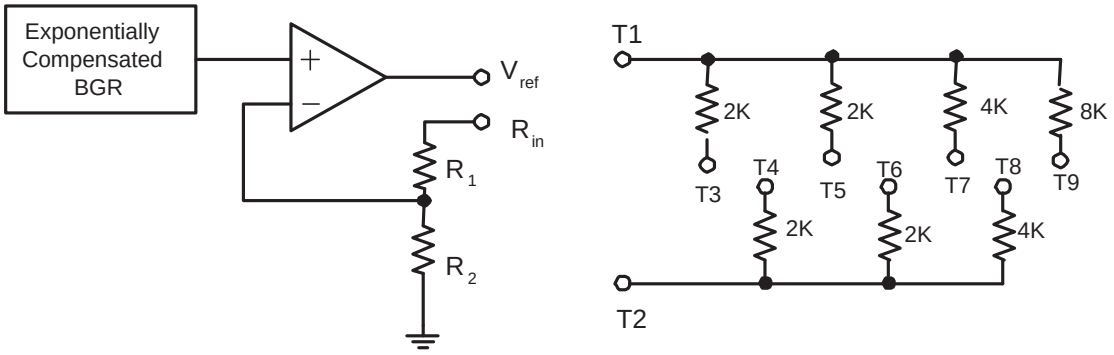

Figure 30: BGR designed for ultra low temperature operation.

voltage of 1.2 V at 37 K, regardless of process and supply variations, the exponential curvature-compensated BGR was placed into a resistive feedback network, as shown in Figure 30. In this circuit, when terminals V_{ref} and R_{in} are shorted, the output voltage is expressed as

$$V_{ref} = V_{out,\text{exp. BGR}}(1 + \frac{R_1}{R_2}), \tag{18}$$

where $V_{out,\text{exp. BGR}}$ is the output voltage from the exponential curvature-compensated BGR circuit.

A resistive network with eight terminals was implemented to allow trimming of the output voltage. The nine terminals of the network are connected to external pins and in case trimming is required, the resistive network can get in series with resistor R_1 with proper external connections to adjust the output voltage to the required value and also to find the optimum value for resistor R_1 for future fabrications.

The core circuit (exponential curvature-compensated BGR) itself, and the final BGR circuit were fully characterized at 37 K. Measurement results for the output voltage of both circuits across a 3600 s time window, are shown in Figure 31. As it can be seen, after stabilization, both circuits function reliably at this temperature and an output voltage of 1.2 V was indeed achievable at 37 K, clearly good news for JWST mission. Resistive network was employed in order to obtain an output voltage of 1.2 V at this extremely low temperature. Measurement results show that with the

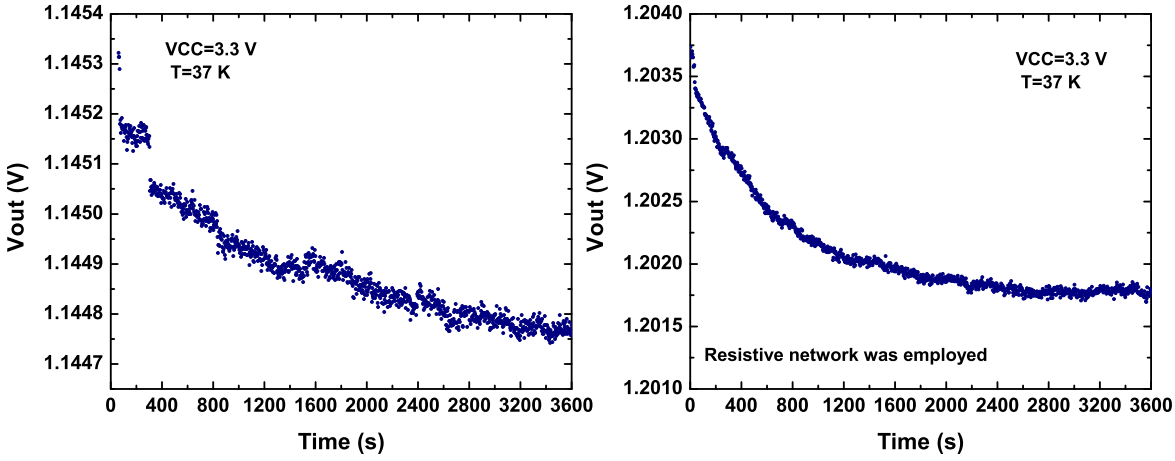

Figure 31: Measured output voltage of the exponential curvature-compensated BGR and its amplified version at 37 K as a function of time.

power supply of 3.3 V, the total power consumption for the core and the final BGR circuits are 128 μW and 248 μW, respectively.

4.3 Summary

In this chapter, we demonstrated the DC measurements of SiGe HBTs operating in environments below 1 K. The SiGe HBTs remain functional, with usable current gains. A SiGe BGR circuit was also fully characterized and verified to operate reliably at sub-1-K temperatures. A voltage reference circuit delivering robust performance at 37 K was successfully designed and fully characterized.

CHAPTER V

THE IMPACT OF PROTON IRRADIATION ON SIGE BGRS

In this chapter, the impact of proton irradiation on the wide-temperature performance of SiGe BGR circuits is investigated. To investigate the effect of technology scaling the SiGe references designed in two SiGe technologies; first- and third-generation technologies are considered. To investigate the impact of temperature and bias during the irradiation, three different radiation experiments are performed. In the first experiment, voltage references from the two SiGe technologies are irradiated under bias at room temperature. For the second experiment, the references from the two SiGe technologies are irradiated cold while under bias, and for the third experiment, one reference from the third-generation SiGe technology is irradiated at room temperature with all pins grounded. Experimental measurements are provided and discussed.

5.1 Experiment

The bandgap voltage references used for this study are the first-order (Figure 11) and the exponential curvature-compensated BGRs (Figure 13) that were described in Chapter 3. Both BGRs were implemented in IBM's 5AM and in IBM's 8HP SiGe BiCMOS technologies. Circuits were mounted onto 28-pin ceramic DIP packages, wire-bonded, and characterized prior to proton irradiation. The samples were irradiated with 63.3 MeV protons at the Crocker Nuclear Laboratory at the University of California at Davis.

To investigate the effects of irradiation temperature, irradiation bias, and technology scaling, the following three experiments were performed:

- Experiment I: The circuits from both SiGe technologies, were irradiated under bias at room temperature. Two different equivalent total doses were used: 600 krad(Si) (a proton fluence of 4.3x10^{12} p/cm^2) and 3 Mrad(Si) (a proton fluence of 2.1x10^{13} p/cm^2).

- Experiment II: The circuits from both SiGe technologies, were inserted into a liquid nitrogen bath and were irradiated under bias at 77 K. The output voltages of the 8HP references were measured at 77 K, during irradiation, at four total dose levels of 300 krad(Si), 600 krad(Si), 1 Mrad(Si) and 3 Mrad(Si). The measured equivalent total dose for the 5AM reference was 3 Mrad(Si).

- Experiment III: The exponential curvature-compensated BGR from the IBM's 8HP SiGe technology was irradiated at room temperature, with all terminals grounded (previously shown to have negligible impact on the radiation response of individual SiGe HBTs [101]). The measured equivalent total dose was 600 krad(Si).

5.2 Results and Discussion

The output voltage of each circuit was measured prior to, and subsequent to irradiation, at different temperatures ranging from -263° C to 27° C. Electrical measurements were performed using an Agilent 4155 Semiconductor Parameter Analyzer. In the following sections, the measurement results of each experiment are discussed.

5.2.1 Experiment I: Irradiation at Room Temperature

Measurement results from Experiment I are shown in Figures 32-36. As mentioned above, in this experiment the samples were irradiated at room temperature while they were under bias. Figure 32 shows the percentage change in the output voltage of the 5AM BGR as a function of temperature for total dose values of 600 krad(Si) and 3 Mrad(Si). Previous studies on the effects of radiation on precision voltage references

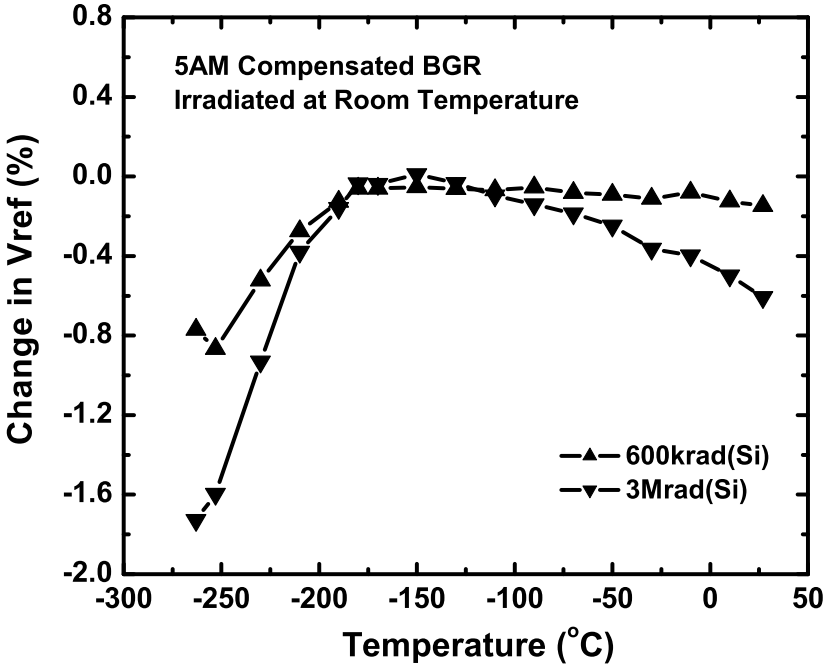

Figure 32: Change in the output voltage of 5AM BGR irradiated at room temperature as a function of temperature.

usually report this percentage change as a function of total dose/proton fluence, but only at room temperature. Here, we have shown these changes down to extremely low temperatures. The percentage change was calculated according to

$$\Delta\text{Vref(T)}(\%) = \frac{\text{Vref}_{\text{post-rad}}\text{(T)-Vref}_{\text{pre-rad}}\text{(T)}}{\text{Vref}_{\text{pre-rad}}\text{(T)}} \times 100. \tag{19}$$

Figure 32 shows that for the case of 3 Mrad(Si) total dose, the percentage change in the output voltage of 5AM BGR is larger than for the case of 600 krad(Si), and the percentage change becomes larger at very low temperatures. To assess what part of circuit plays the role in causing the value of the output voltage to change after the reference was irradiated, the base-emitter voltage of transistor Q_3 and the base-emitter voltage difference of transistors Q_1 and Q_2 were measured both before and after irradiation and their percentage changes have been plotted in Figures 33

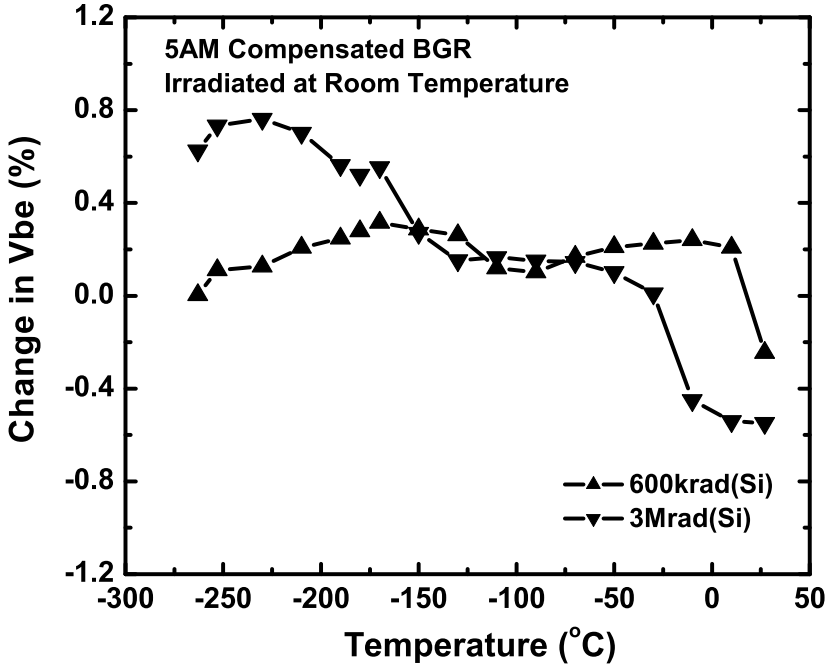

Figure 33: Change in the base-emitter voltage of Q_3 inside 5AM BGR irradiated at room temperature as a function of temperature.

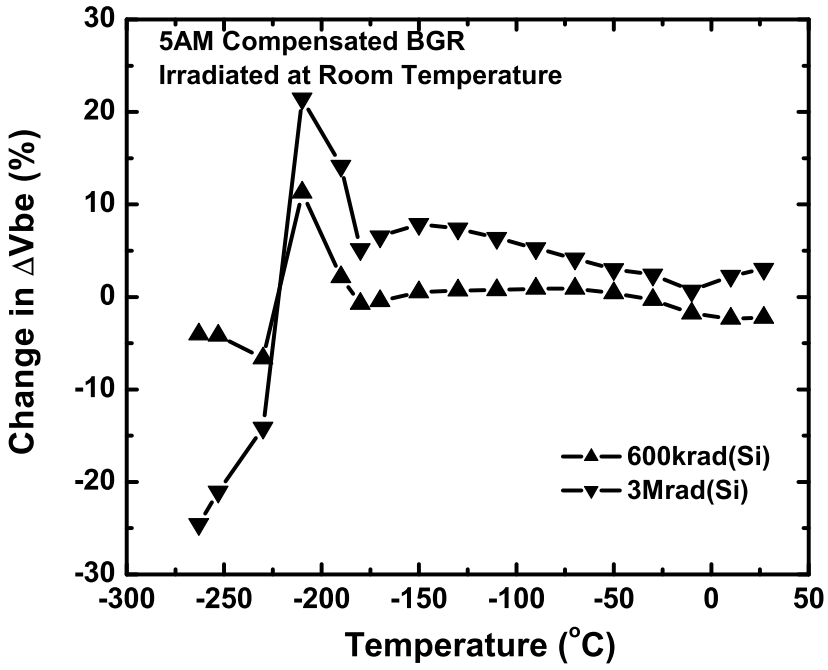

Figure 34: Change in the difference of Q_1 and Q_2 base-emitter voltages of 5AM BGR irradiated at room temperature as a function of temperature.

and 34, respectively. One can see that the percentage change in the base-emitter voltage difference is much larger than the percentage change in the base-emitter voltage, indicating that the PTAT current generator likely plays the main role in causing the output voltage to change following irradiation. For this PTAT current generator section to operate properly, the current in the two branches should remain equal. Any mismatches between the large and small area transistors in these two branches can degrade the overall performance of the circuit and measurement results confirms this assumption. The line regulation was also measured and it was observed that it remains well-behaved across the extreme temperature range before and after irradiation.

Figures 35 and 36 show the percentage change in the output voltages of the 8HP first-order and curvature-compensated BGRs, respectively, for total dose values of 600 krad(Si) and 3 Mrad(Si). From the data, it can be seen that the circuits function well down to temperatures as low as -263° C. It can be observed that the proton-induced changes in the BGR are minor, even at cryogenic temperatures. Comparing the effects of proton radiation on the circuits for the two SiGe technologies, we can see that 5AM references are generally more susceptible to radiation damage than 8HP references, consistent with the overall TID robustness of the individual transistors [51].

5.2.2 Experiment II: Irradiation at 77 K

In this experiment, the effects of proton irradiation on the voltage references implemented in both SiGe technologies were investigated when irradiated cold. The samples were irradiated at 77 K and under operational bias during the experiment. Measurement results are shown in Figures 37-42. In each figure, the radiation performed at room temperature is also shown for comparison. The percentage change in the output voltage of the 5AM BGR is shown in Figure 37. It can be observed that

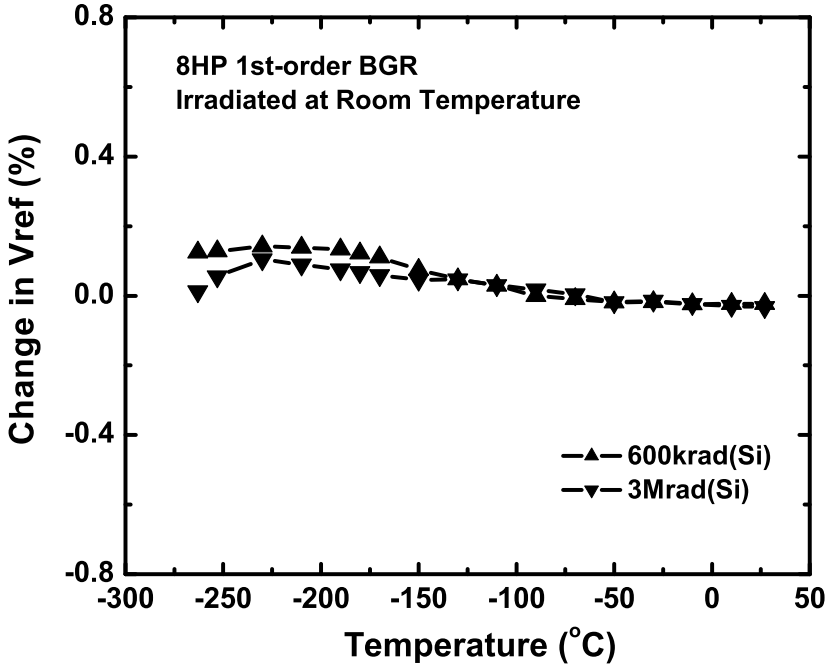

Figure 35: Change in the output voltage of 1st-order 8HP BGR irradiated at room temperature as a function of temperature.

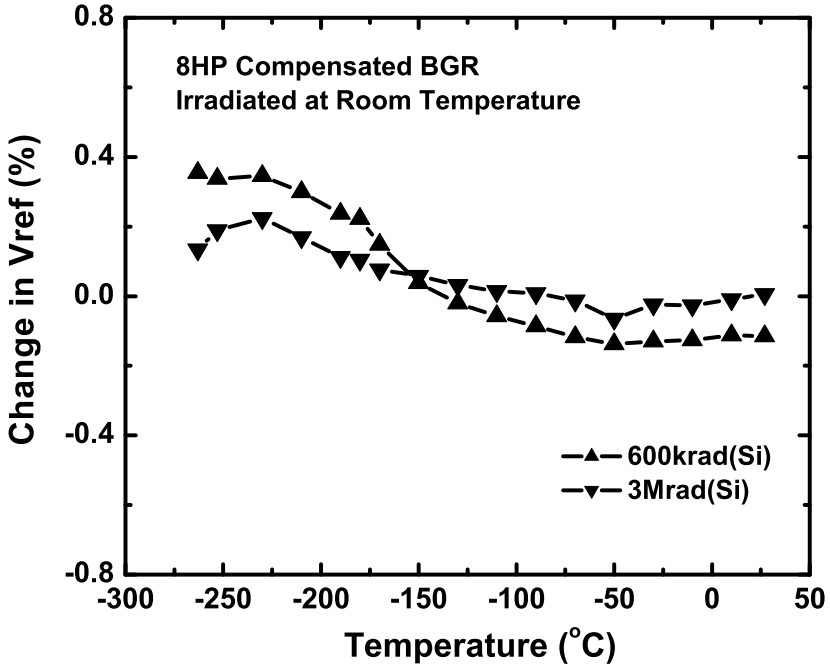

Figure 36: Change in the output voltage of curvature-compensated 8HP BGR irradiated at room temperature as a function of temperature.

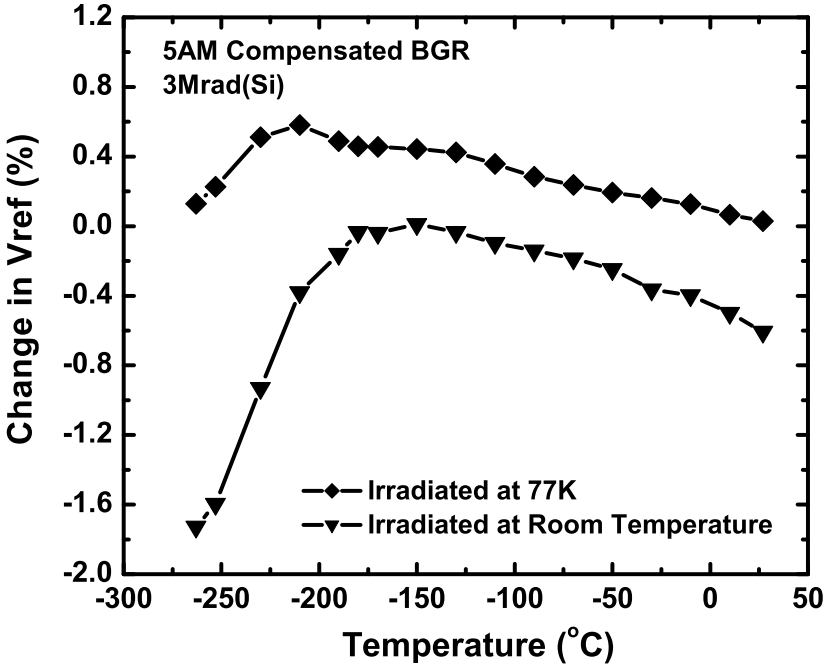

Figure 37: Change in the output voltage of 5AM BGR irradiated at 77 K as a function of temperature.

the change in the output voltage, when the reference is irradiated cold, is much less than when it is irradiated at room temperature, clearly good news for applications at cryogenic temperatures. This is consistent with what was observed for the individual transistors [49]. Figure 38 shows that the percentage change in the base-emitter voltage of transistor Q_3 is less than 0.5 % when the reference is irradiated at 77 K. The percentage change in the base-emitter voltage difference of transistors Q_1 and Q_2 is shown in Figure 39. It can be seen that for most temperatures the percentage change remains the same for both samples (irradiated at room temperature and irradiated at 77 K). Interestingly, however, at deep cryogenic temperatures, the percentage change in ΔV_{be} for the sample irradiated at room temperature is far larger than that of the sample irradiated cold. The percentage change of the output voltages of the 8HP references as a function of total dose at 77 K are plotted in Figure 40. As it can be

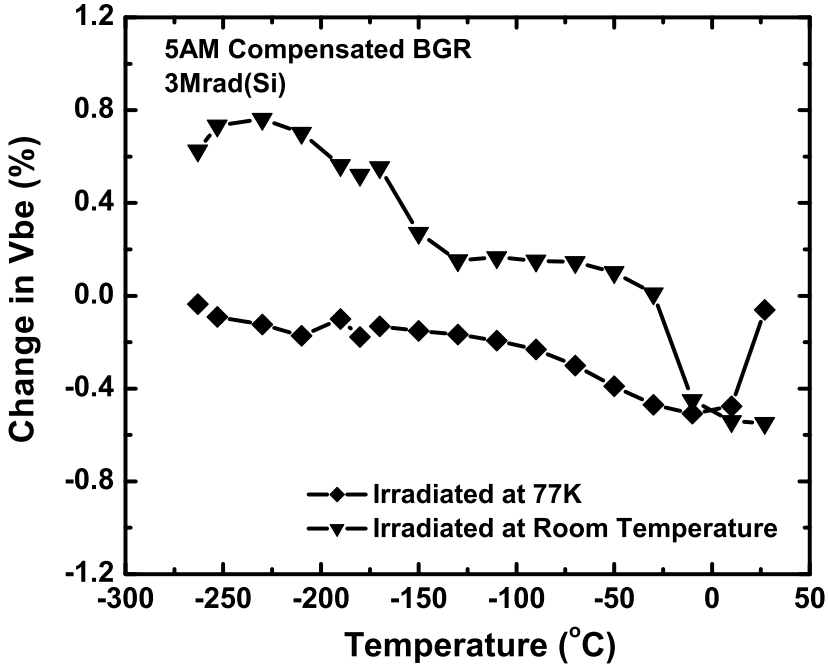

Figure 38: Change in the base-emitter voltage of Q_3 inside 5AM BGR irradiated at 77 K as a function of temperature.

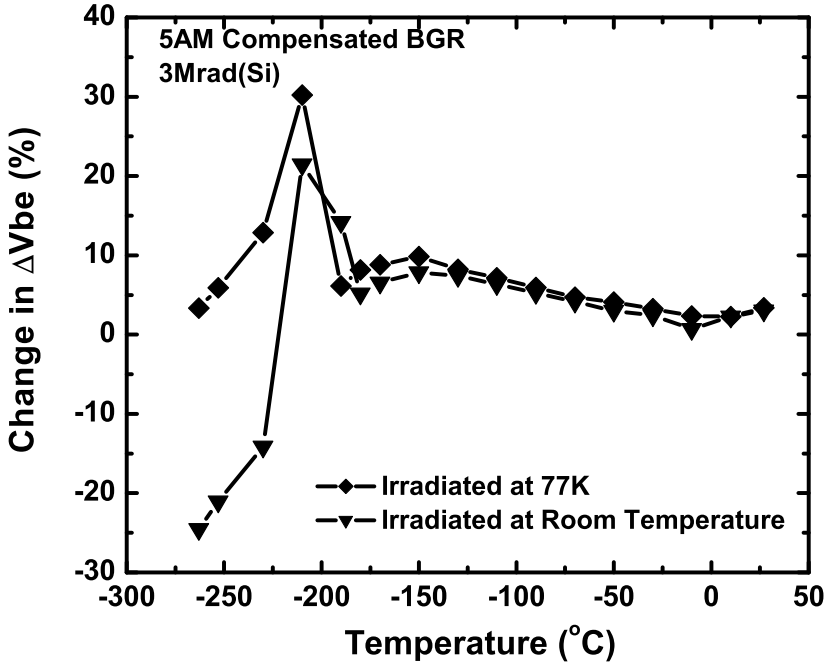

Figure 39: Change in the difference of Q_1 and Q_2 base-emitter voltages of 5AM BGR irradiated at 77 K as a function of temperature.

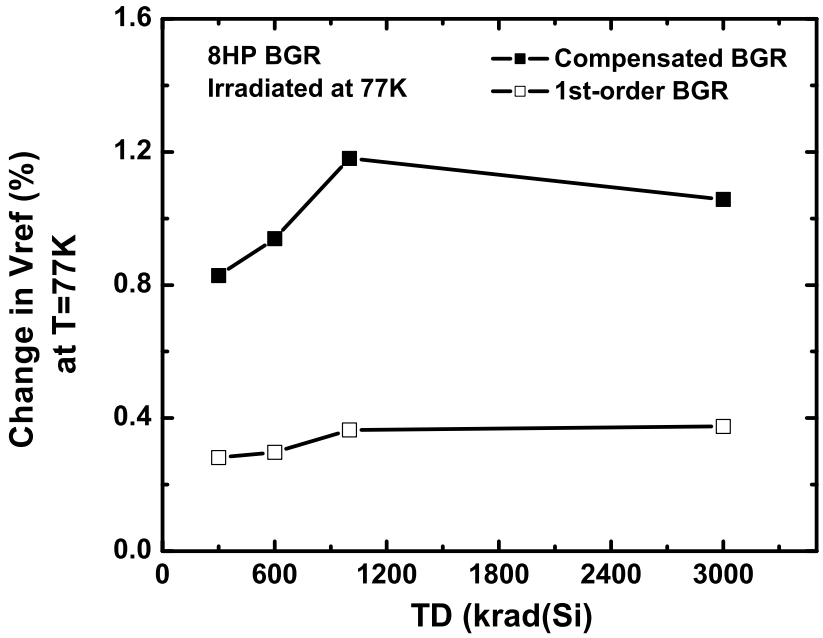

Figure 40: Output voltage of 8HP references as a function of total dose for 77 K irradiation.

seen, the percentage change increases as the total dose increases. The change in the output voltage of the first-order and curvature-compensated 8HP BGRs irradiated at 77 K as a function of temperature are shown in Figures 41 and 42, respectively. Unlike the case of the 5AM references, the output voltage of the 8HP samples irradiated at 77 K changed more after irradiation compared with the samples irradiated at room temperature. However, the percentage change for both 8HP references is less than 0.4 %, clearly acceptable for most applications.

Table 5: Temperature coefficients of 5AM SiGe Voltage Reference over Different Temperature Ranges.

Temperature Range	Experiment I		Experiment II	
	pre-rad	post-rad (3 Mrad(Si))	pre-rad	post-rad
(-55 to 27)° C	19.52 ppm/° C	27.45 ppm/° C	8.06 ppm/° C	19.22 ppm/° C
(-180 to 27)° C	72.29 ppm/° C	55.11 ppm/° C	64.61 ppm/° C	49.99 ppm/° C
(-243 to 27)° C	96.29 ppm/° C	168.83 ppm/° C	101.66 ppm/° C	88.08 ppm/° C
(-263 to 27)° C	122.37 ppm/° C	167.51 ppm/° C	120.63 ppm/° C	121.52 ppm/° C

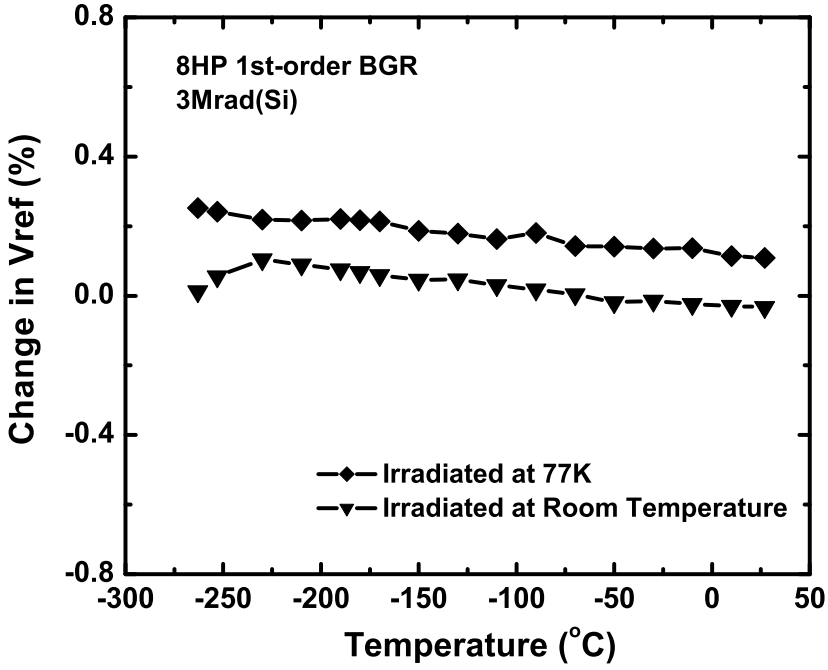

Figure 41: Change in the output voltage of the first-order 8HP BGR irradiated at 77 K as a function of temperature.

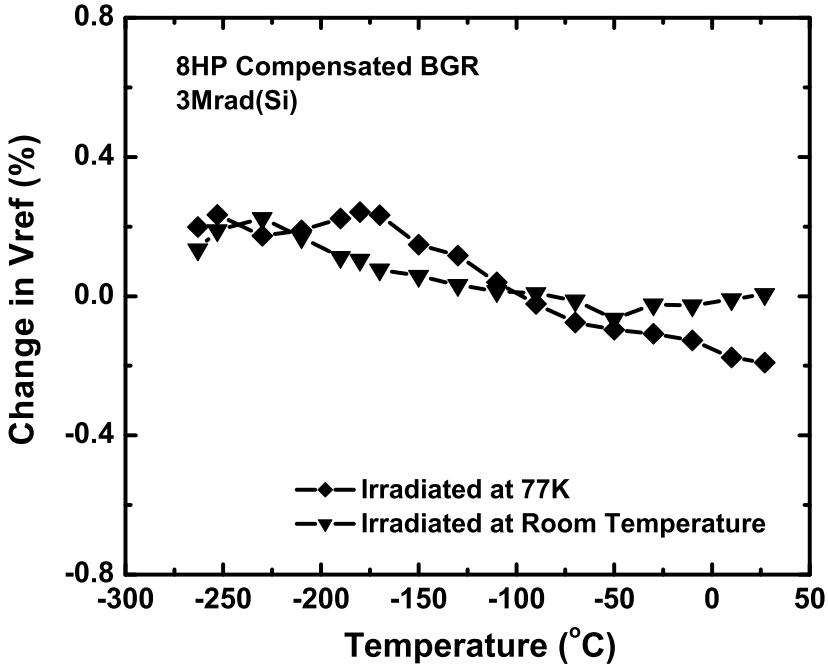

Figure 42: Change in the output voltage of curvature-compensated 8HP BGR irradiated at 77 K as a function of temperature.

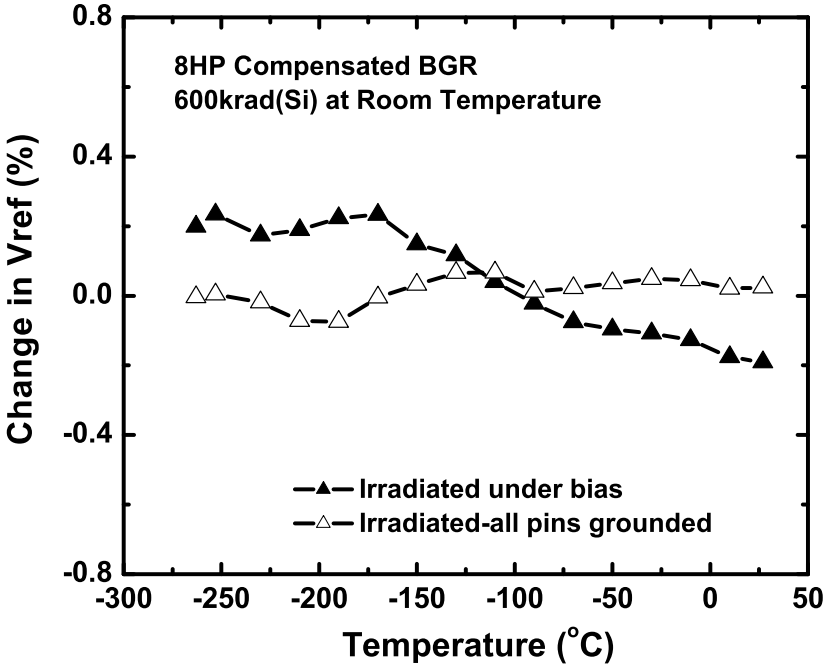

Figure 43: Change in the output voltage of curvature compensated 8HP BGR irradiated with all pins grounded, as a function of temperature.

5.2.3 Experiment III: Irradiation with all pins grounded

In this experiment, the 8HP curvature-compensated reference was irradiated at room temperature with all the pins grounded. Measurement results of this experiment are shown in Figure 43. Data obtained from experiment I is also shown for comparison. Interestingly, these results indicate the proton damage for this reference is larger for the case when the circuit is under bias during radiation, compared to the case when the circuit is irradiated with all pins grounded, and is different than the response for the individual transistors, where grounded operation is generally found to be worst case.

The temperature coefficients of the 5AM voltage reference both before and after irradiation from the two experiments, across four different temperature ranges, are

summarized in Table 5. These numbers demonstrate that the impact of proton irradiation at 77 K on the output voltages and temperature coefficients of the 5AM BGR circuit are minor, and are clearly encouraging for extreme environment applications of SiGe technology.

5.3 Summary

In this chapter, proton tolerance of SiGe BiCMOS voltage references intended for extreme temperature range electronics was investigated. The reference circuits were designed in two distinct SiGe technologies (IBM SiGe 5AM and IBM SiGe 8HP). Three separate proton radiation experiments were performed. Measurement results show that the PTAT current generator inside the reference circuits is the most vulnerable component of the circuits to induce proton damage, but in general the circuits work well up to Mrad levels of total dose. The output voltage of the 5AM reference circuits show larger percentage changes than those of the 8HP references, after irradiation at room temperature. Irradiation at 77 K produces less damage to the 5AM reference circuits than irradiation at room temperature. For the 8HP reference circuits, the damage of radiation at 77 K was slightly larger than the damage of radiation at room temperature, but still relatively minor. Comparing the measurement results at 27° C obtained from this study, with those of previous studies [102]-[104], indicates that the output voltage change due to proton influence is minimal in the SiGe BGR circuits, even down to cryogenic temperatures.

CHAPTER VI

THE IMPACT OF X-RAY IRRADIATION ON SIGE BGRS

Proton radiation response of SiGe BGRs was studied in the previous chapter and only minor changes in the SiGe BGR performance up to total ionization dose (TID) of 3 Mrad(Si) was observed. In this chapter, we investigate the effects of irradiation source on the performance of BGR circuits. At the transistor level, differences in the degradation induced by 10 keV x-rays and 63.3 MeV protons have been observed [105], [106], which provides a clear motivation to determine if these source dependent differences will be encountered at the circuit level as well, affecting the overall circuit performance.

This chapter is organized as follows. We first present a comprehensive investigation of the performance dependencies of irradiated SiGe BGR circuits on TID level and radiation source. Two types of SiGe BGR circuits were designed and exposed to x-rays at two different TID levels, 1,080 krad(SiO_2) and 5,400 krad(SiO_2). Degradation due to 10 keV x-rays is shown to be dependent on both the TID level and the circuit topology. The origins of these dependencies are investigated and explained through detailed circuit analysis. To investigate the effects of radiation source on circuit performance, the circuit topology showing the worst-case degradation from the x-ray experiment was exposed to 63.3 MeV protons to the same effective TID level. Measurement results from proton irradiation are compared with those from the x-ray experiment and it is shown that circuit response is indeed radiation source dependent. Possible explanations for this observation are discussed.

6.1 Experiment

To better understand the effects of irradiation on the performance of SiGe voltage references, two different BGR circuit topologies, namely the first-order BGR (or uncompensated BGR shown in Figure 11), and the exponential curvature-compensated BGR (shown in Figure 13) implemented in IBMs SiGe 5AM BiCMOS technology platform, and as described in Chapter 3, were selected. The BGR circuits and along with 5AM HBT transistors were mounted onto 28-pin ceramic DIP packages, wirebonded, and fully characterized both prior to, and subsequent to irradiation. A closed-cycle helium cryostat was used for characterization over temperature. X-ray irradiation was performed at Vanderbilt University using an ARACOR x-ray test system. Circuits under operating bias and devices in forward-active bias configuration were irradiated at room temperature with 10 keV x-rays to total ionizing doses (TID) of 1,080 krad(SiO_2) and 5,400 krad(SiO_2), at the dose rate of 60 krad(SiO_2)/min. All electrical measurements were performed using an Agilent 4155 Semiconductor Parameter Analyzer.

6.2 X-Ray Irradiation

The output voltages of the two SiGe BGR circuits were measured before and after x-ray irradiation, at different temperatures ranging from 27° C down to -230° C. Measurement results are shown in Figures 46-49. Figures 46 and 47 show the output voltage of the first-order BGR and the compensated BGR, respectively, before and after irradiation to total dose value of 1,080 krad(SiO_2). As it can be seen, a small shift in the output voltage of the compensated BGR is observed across temperature after irradiation. The change in the output voltage of the first-order circuit is almost negligible after x-ray exposure. These figures show that both circuits are quite robust to x-ray exposures up to 1,080 krad(SiO_2). The output voltage of the first-order and the compensated BGRs before and after x-ray irradiation at a TID level of 5,400

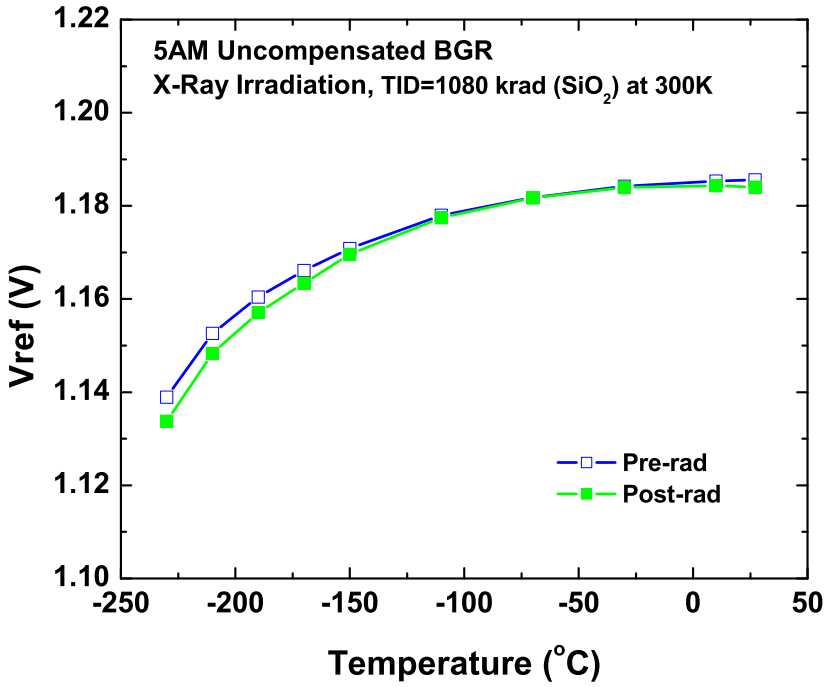

Figure 44: Output voltage of uncompensated BGR before and after x-ray irradiation with TID = 1,080 krad(SiO_2).

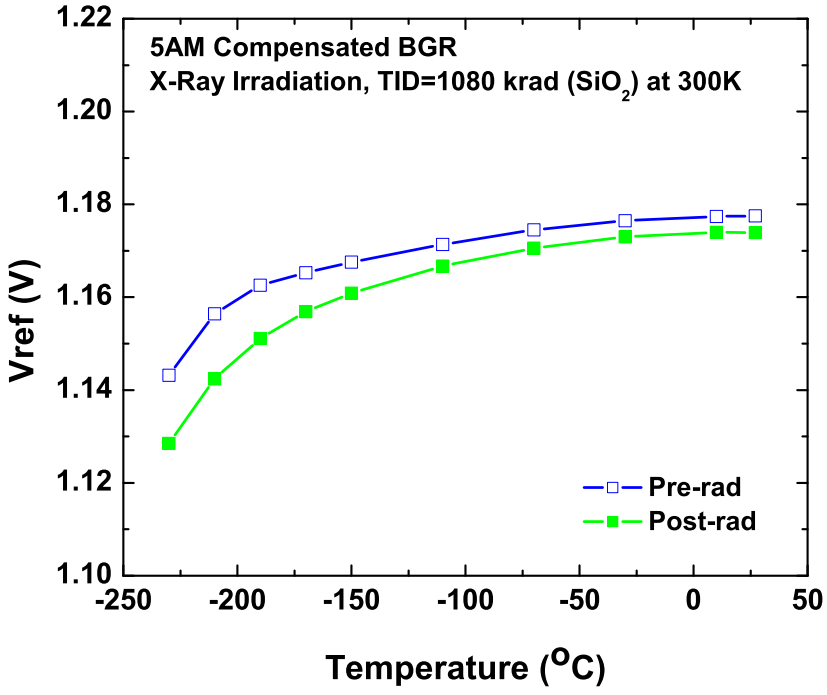

Figure 45: Output voltage of compensated BGR before and after x-ray irradiation with TID = 1,080 krad(SiO_2).

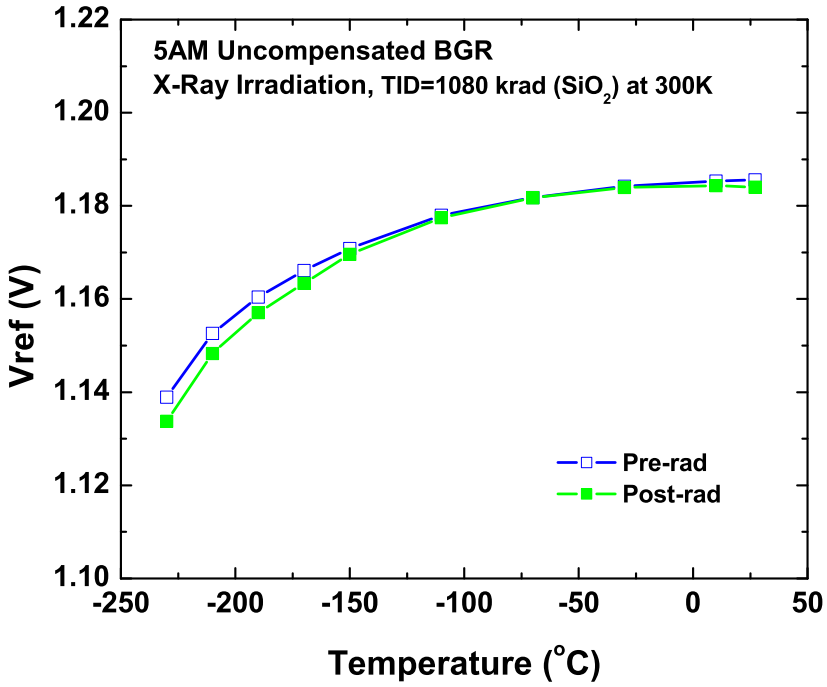

Figure 46: Output voltage of uncompensated BGR before and after x-ray irradiation with TID = 1,080 krad(SiO_2).

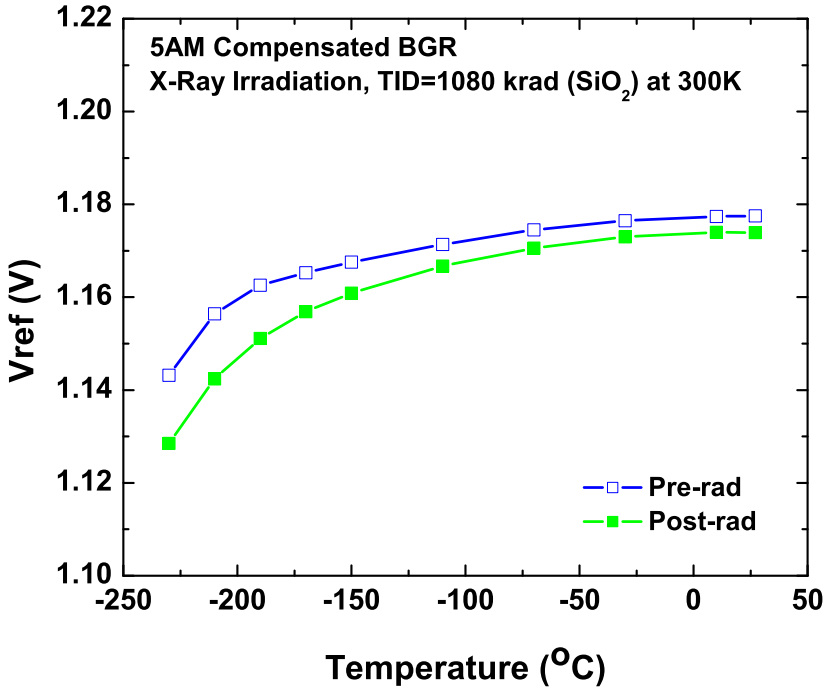

Figure 47: Output voltage of compensated BGR before and after x-ray irradiation with TID = 1,080 krad(SiO_2).

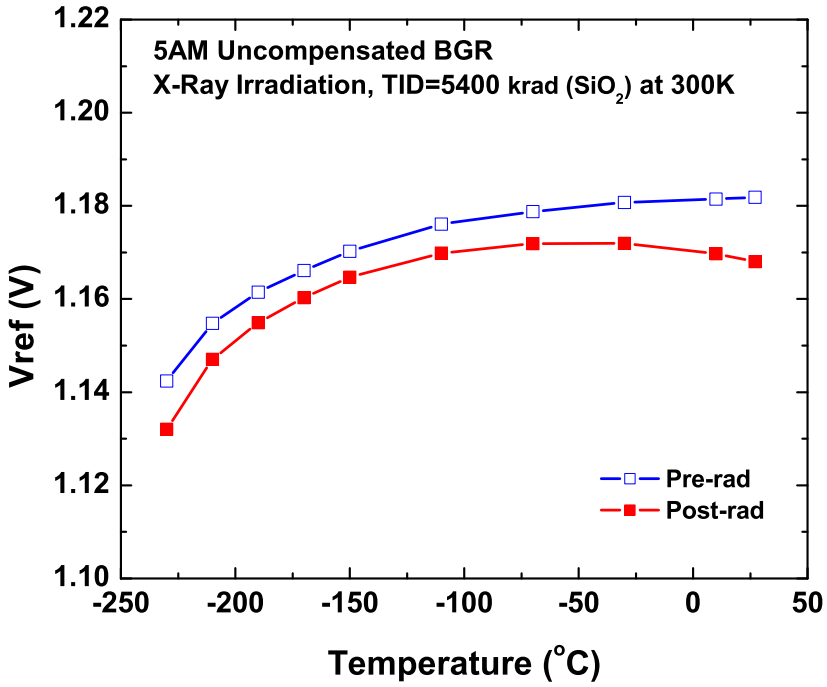

Figure 48: Output voltage of uncompensated BGR before and after x-ray irradiation with TID = 5400 krad(SiO_2).

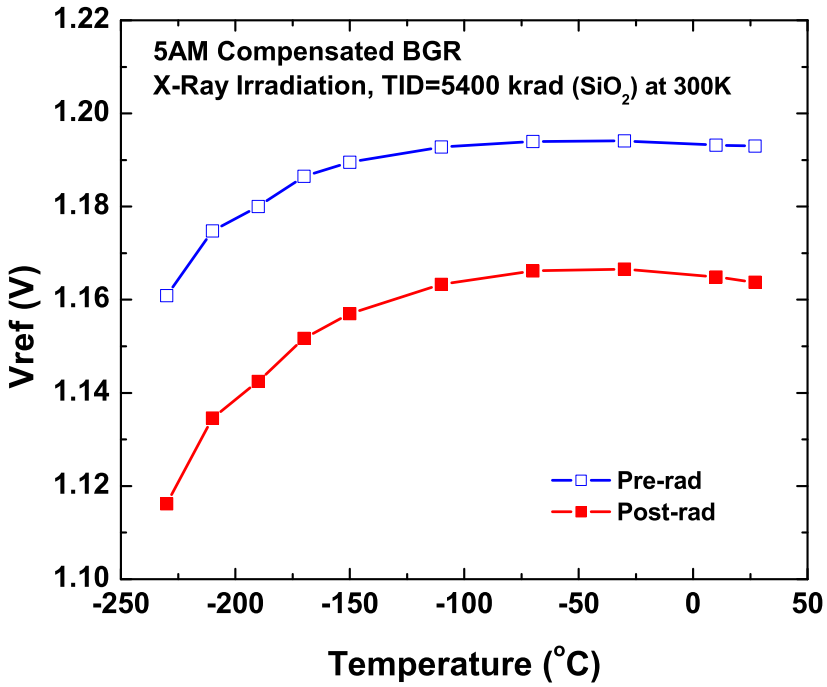

Figure 49: Output voltage of compensated BGR before and after x-ray irradiation with TID = 5,400 krad(SiO_2).

krad(SiO_2) is shown in Figures 48 and 49, respectively. Unlike the previous case, the output voltage of both circuits show significant degradation across all temperatures. This shift in the output voltage is more visible in the compensated BGR than in the first-order BGR. Table 6 summarizes the performance metrics of the two SiGe BGR circuits before and after x-ray irradiation to total dose values of 1,080 krad(SiO_2) and 5,400 krad(SiO_2). Note that the circuits used for the two TID exposure experiments are from two different dies, and the difference among the pre-rad performance metrics is attributed to the on-wafer process variations. The observed degradation in the output voltage of the BGR circuits due to exposure to high dose x-rays could be potentially an important issue for certain extreme-exposure applications (e.g., outer planet exploration), since BGR circuits are widely used, and often embedded inside sensitive circuits such as data converters, where their individual block-level response may be masked. Therefore, it is important to understand the origins that cause the observed output voltage anomalies.

6.2.1 Discussion

To identify the origins of degradation in the output voltage of SiGe BGR circuits after exposure to high-dose x-rays, we need to carefully examine the two circuit topologies and understand what parameters actually contribute to generating the output voltage. We first start with the first-order BGR circuit, shown in Figure 11. As it can be seen from equation (9), the base-emitter voltage of transistor Q_3 and the current I_{ref} are the main contributers to the magnitude of the output voltage. Note that the value of the resistor R_2 is 7.4 kΩ and as a result a small shift of 2 μA in the magnitude of the current I_{ref} will change the magnitude of the output voltage by almost 15 mV. The base emitter voltage of transistor Q_3 was measured prior to, and subsequent to irradiation over temperature while the circuit was under operation. The results are plotted in Figure 50. This Figure shows that even for a high TID level of 5,400

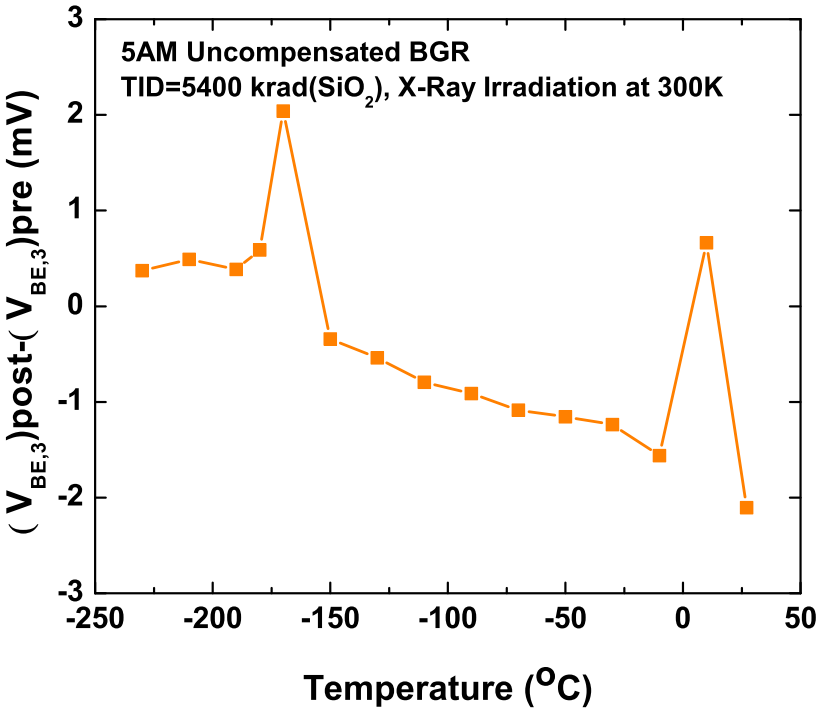

Figure 50: Change in the difference of Q_1 and Q_2 base-emitter voltages of 5AM SiGe BGR irradiated at room temperature as a function of temperature.

krad(SiO_2), the change in the base-emitter voltage of transistor Q_3 across temperature is small (typically less than 2 mV) after irradiation, suggesting that the term $V_{BE,3}$ does not contribute to the observed TID dependent output voltage anomalies. The presence of the two spikes in this Figure could be attributed to measurement error, as they occur at only two temperature points (0° C and -170° C, well far from each other). Therefore, we can conclude that I_{ref} is the major contributor to the output voltage degradation of the BGR circuit. As it can be seen from Figure 11, I_{ref} is the amplified version of I_{PTAT} which is given in (7). In deriving (7), it has been assumed that the base current is negligible. However, as it has been discussed in [105], [106], the base leakage current increases after x-ray radiation and therefore,

cannot be neglected after exposures to these dose levels. The increase in the post-irradiation base current is due to the creation of positive charge in the emitter-base (EB) oxide spacer and increase in the number of traps at the EB spacer oxide/silicon interface, which results in increased surface recombination velocity [107]. To show this, four parallel copies of $0.5 \times 2.5\ \mu m^2$ device, similar to transistors Q_1 and Q_3 in the first-order BGR, were laid out, fabricated and measured prior to, and subsequent to x-ray irradiation. The radiation experiment was performed while the transistors were under bias in the forward-active region. Figure 51 shows the measured Gummel characteristics of such a device at three different temperatures, before and after x-ray irradiation. As expected, Figure 51 indicates that the base current increases as the TID level increases. The current gain of this transistor as a function of collector current is shown in Figure 52, indicating that the current gain significantly degrades after exposure to TID level of 5,400 krad(SiO_2), specially when the transistor is biased in the low bias region. This is indeed the case with all of the SiGe HBTs in both BGR circuits, since at room temperature, they are all biased in the $(25 - 50)\ \mu$A region. We thus continue the circuit analysis of the first-order BGR taking into account the base currents of both transistors Q_1 and Q_2. In this case, the I_{PTAT} current can be expressed as

$$I_{PTAT} = \frac{V_T}{R_1} \ln[(1 - \frac{2}{\beta})\frac{A_2}{A_1}] - IB_{Q2}, \tag{20}$$

where, V_T is the thermal voltage, β is the current gain, $\frac{A_2}{A_1}$ is the emitter area ratio of transistors Q_2 and Q_1 (equal to 8 in both BGR circuits), and IB_{Q2} is the base current of transistor Q_2. Equation (20) shows that any change in IB_{Q2} or β will directly affect the magnitude of I_{PTAT}. Note that any change in I_{PTAT} is multiplied by a factor of kR_2 and could cause a significant shift in the output voltage. This could in fact explain the observed TID dependence of output voltage degradation (Figures 46 and 48). A radiation-induced increase in the base current and the consequent degradation of the current gain is much smaller for the TID level of 1,080 krad(SiO_2)

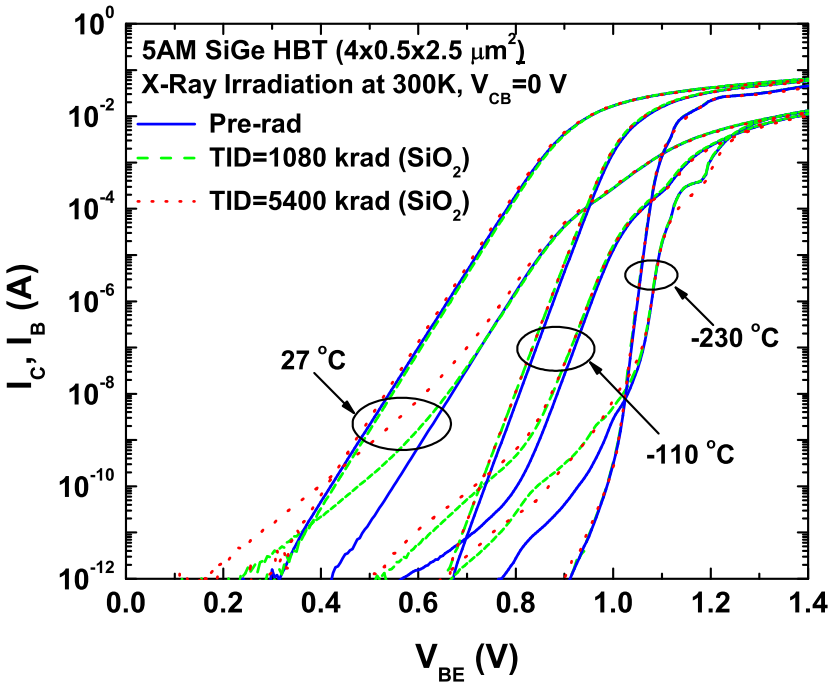

Figure 51: Gummel characteristics before and after x-ray irradiation with TID levels of 1,080 and 5,400 krad(SiO_2).

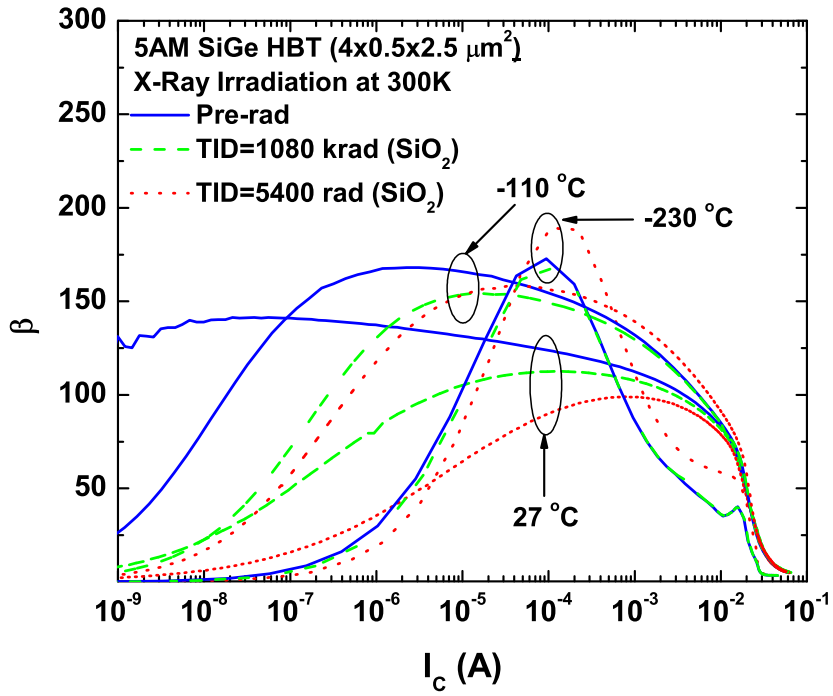

Figure 52: Current gain before and after x-ray irradiation with TID levels of 1,080 and 5,400 krad(SiO_2).

Table 6: Performance metrics of SiGe BGRs before and after x-ray irradiation.

BGR Circuit	V_{ref} (V)		I_{cc} (μA)		TC (ppm/° C) (-180 : 27)° C		TC (ppm/° C) (-70 : 27)° C	
	pre-rad	post-rad	pre-rad	post-rad	pre-rad	post-rad	pre-rad	post-rad
Uncompensated (1080 krad(SiO_2))	1.186@27° C 1.163@-180° C	1.184@27° C 1.160@-180° C	113.0@27° C 51.4@-180° C	113.7@27° C 47.9@-180° C	90.3	98.0	33.08	22.6
Compensated (1080 krad(SiO_2))	1.177@27° C 1.164@-180° C	1.174@27° C 1.154@-180° C	129.9@27° C 55.3@-180° C	130.1@27° C 52.1@-180° C	55.6	82.7	26.3	29.3
Uncompensated (5400 krad(SiO_2))	1.182@27° C 1.164@-180° C	1.168@27° C 1.158@-180° C	115.6@27° C 52.7° C@-180	109.1@27° C 44.3@-180° C	73.5	65.4	26.2	34.1
Compensated (5400 krad(SiO_2))	1.193@27° C 1.186@-180° C	1.164@27° C 1.152@-180° C	136.9@27° C 67.6@-180° C	132.4@27° C 52.7@-180° C	39.6	74.1	10.1	25.17

than for 5,400 krad(SiO_2) (Figures 51-52) and therefore, according to equation (20), it is expected that the shift in the output voltage becomes smaller when the circuit is exposed to TID levels of lower than 5,400 krad(SiO_2), consistent with our data.

For the compensated BGR circuit, it is observed that the change in the magnitude of the output voltage is much larger compared to that of the first-order BGR, after x-ray radiation exposure. This observation can also be explained by analyzing the circuit and explicitly taking into account base current effects. As discussed in Chapter 3, the output voltage of this circuit is given by (13). The current I_{ref} is equal to the summation of the collector current of transistor Q_5, IC_{Q5}, and the base current of transistor Q_3, IB_{Q3}. Transistors Q_1 and Q_5 are identical pairs and therefore,

$$IC_{Q5} = IC_{Q1} = I_{PTAT} - IB_{Q1} - IB_{Q2} - IB_{Q5} \tag{21}$$

where IB_{Q1}, IB_{Q2} and IB_{Q5} represent the base currents of transistors $Q1$, $Q2$ and $Q5$, respectively. Similar to the analysis presented for the first-order BGR, the current I_{PTAT} in Figure 13 can then be expressed as

$$I_{PTAT} = \frac{V_T}{R_1} \ln[(1 - \frac{3}{\beta})\frac{A_2}{A_1}] - IB_{Q2}. \tag{22}$$

Using (21) and (22) in (13), the output voltage of the compensated BGR can be written as

$$\begin{aligned} V_{ref} = V_{BE,3} &+ R_2(\frac{V_T}{R_1} \ln[(1 - \frac{3}{\beta})\frac{A_2}{A_1}]) \\ &+ R_2(-2IB_{Q2} - IB_{Q1} - IB_{Q5} + IB_{Q3}). \end{aligned} \tag{23}$$

Assuming identical base currents for all the transistors, (23) can be simplified as

$$V_{ref} = V_{BE,3} + R_2(\frac{V_T}{R_1}\ln[(1-\frac{3}{\beta})\frac{A_2}{A_1}] - 3IB_{Q2}). \quad (24)$$

Equation (24) shows that any change in the base current after irradiation results in almost a 3× shift in the magnitude of the output voltage in the compensated BGR than in the first-order BGR. Also note that the value of resistor R_2 used in the compensated BGR is twice as large as the one used in the first-order BGR.

The discussion provided in this section clearly explains the reasons behind the observed sensitivity of the output voltage to both TID level and circuit topology. To prevent the post-irradiation degradation of the performance of these voltage references, circuit techniques need to be developed to minimize the dependency of the output voltage on the base current of the SiGe HBTs.

6.3 Proton vs X-ray Irradiation

The results of the effects of proton irradiation on the performance of SiGe BGRs studied in the previous chapter illustrated that proton-induced changes in the SiGe BGR circuits are minor up to a TID level of 3 Mrad(Si). However, in the previous section, it was shown that x-ray irradiation at high TID level of 5,400 krad(SiO_2) can significantly degrade the performance of the BGR circuits. To investigate the impact of radiation source on the performance of SiGe voltage references, the compensated BGR which showed worse-case performance degradation under x-ray exposure, was irradiated to the same effective TID level of 5,400 krad(SiO_2) using 63 MeV protons. Note that in the case of 63.3 MeV protons, the equilibrium dose in Si and SiO_2 differ by less than 5%. The 63.3 MeV proton irradiation was performed at the Crocker Nuclear Laboratory at the University of California at Davis. The circuit was irradiated while under operating bias to a TID level of 5,400 krad(SiO_2).

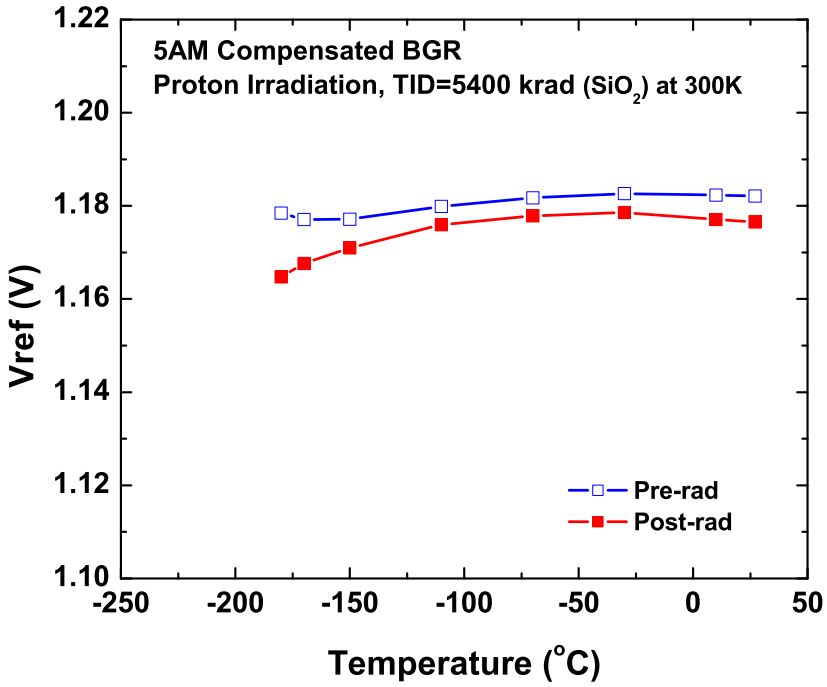

Figure 53: Output voltage of compensated BGR before and after proton irradiation at 300 K with TID = 5,400 krad(SiO_2).

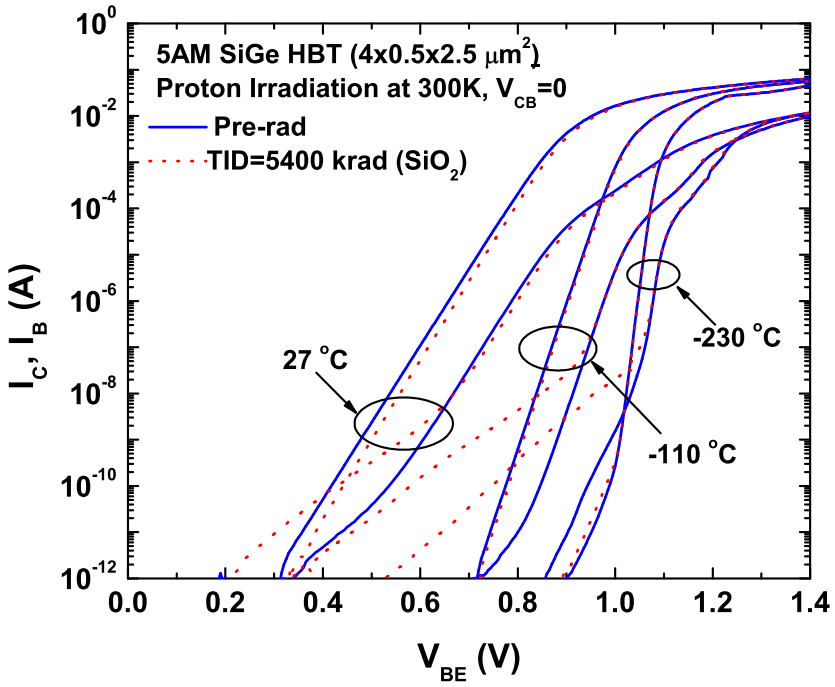

Figure 54: Gummel characteristics before and after proton irradiation at 300 K with TID = 5,400 krad(SiO_2).

6.3.1 Discussion

Measurement results prior to and subsequent to proton irradiation are illustrated in Figure 53, showing that the output voltage of the compensated BGR has been lowered across temperature by less than 10 mV. Similar to the discussion given in the previous section, this post-rad degradation in the performance could be due to the fact that the base current of SiGe HBTs increases after proton irradiation. Figure 54 shows the Gummel characteristics of the 5AM device at three different temperatures, before and after proton irradiation. This figure indicates that the base current leakage increases after proton irradiation for all three temperatures, and therefore, and according to (24), the magnitude of the output voltage should drop after irradiation, consistent with the data.

A comparison of Figures 49 and 53 indicates that the degradation in the circuit performance is radiation source dependent and proton irradiation shows less degradation than x-ray irradiation. This difference could be attributed to the fact that at the transistor level, the increase in the base leakage current is smaller for protons than for x-rays, as discussed in [105],[106]. This is also observed by comparing Figures 51 and 54 which show that at the base-emitter voltage of 0.7 V, and at room temperature, the base current after x-ray exposure changes by almost 100 nA, while it changes by less than 20 nA after proton irradiation (at the same effective dose). This difference in the degradation induced by x-rays and protons, as discussed in [105], may lie in dose enhancement effects, as low energy x-rays pass through high-Z materials such as the copper layers and the tungsten vias of the metal interconnections.

6.4 Conclusion

In this chapter, we presented a comprehensive investigation of the performance dependencies of irradiated SiGe voltage reference circuits on TID level, circuit topology, and

radiation source. Two different SiGe bandgap voltage reference topologies were designed and exposed to x-rays at TID levels of 1,080 krad(SiO_2) and 5,400 krad(SiO_2). The degradation in circuit performance after x-ray irradiation was observed to be dependent on both the circuit topology, and the TID level. X-ray exposure to large TID levels significantly decreased the magnitude of the output voltage. Explanations for the observed anomalies were provided using detailed analysis of the two circuit topologies. It was found that the excess base leakage current is the primary factor that affects post-irradiation performance degradation. The circuit topology that showed the worst-case degradation from the x-ray experiment was irradiated with 63.3 MeV proton at 5400 krad(SiO_2) TID. Proton and x-ray post-rad circuit responses were compared. At the same TID level, x-ray irradiation was shown to degrade the circuit performance more than proton irradiation. This radiation-source dependence was also attributed to differences in the excess base current leakage. The results presented in this chapter show that ultra-high-dose irradiation can significantly degrade the performance of precision voltage references implemented in SiGe technology. To prevent post-irradiation performance degradation, circuit topologies have to be carefully chosen and circuit techniques need to be applied to minimize the dependency of the output voltage on the transistor base current.

CHAPTER VII

SINGLE-EVENT TRANSIENT EFFECTS IN SIGE BGRS

Single-event transients can originate when high energy particles interact with sensitive structures in a circuit and deposit sufficient energy to generate electron-hole pairs near critical electrical nodes of the device. During SETs, the corresponding injected charge carriers can appear in the form of either voltage or current spikes (or both), which are then able to propagate from the device through the circuit to the system, resulting in transient excursions, data corruption, and eventually system failure. Since first reported in 1993 in operational amplifiers (opamps) and voltage comparators [108], the SET response of different types of circuits (mostly COTS products) have been investigated through a variety of beam experiments, and device/circuit simulations [109]-[124]. When the SET response of a particular circuit is determined, usually under a specific operating condition, one may not be able to use this response to predict the SET response of a system where the circuit is used as a subsystem. Therefore, SET effects continue to be a growing concern for space electronics. This is due to the fact that the amplitude and the duration of SETs depend on several factors, including output load, dynamic nodal impedances, operating conditions, and the nature of the radiation environment [125].

As it was discussed in Chapter 2, with regard to single-event effects, SiGe HBTs lack immunity, and require mitigation techniques that can be accomplished at the circuit level [53], or at the device level [23], or both. As a result, one might expect that the SiGe analog circuits will not be immune to transient effects. In this chapter, we answer the question of how the transients appearing in SiGe HBTs propagate through a SiGe BGR circuit. The BGR circuit is used to provide the input reference

voltage to a voltage regulator. HBTs in the BGR circuit are struck by heavy ions during microbeam experiments, and the subsequent transient responses at the output of the regulator are captured. These results are presented and explained.

7.1 Experiment

In this work, the IBM's 5AM SiGe BiCMOS technology is selected. Proton tolerance, laser induced current transients, and single-event upset mechanisms of the 5AM SiGe HBTs have been reported in [49],[52], [122]. Figure 55 shows the schematic of the voltage regulator used for this study. An exponential curvature-compensated BGR (Figure 13) was used to provide the reference voltage to the regulator. The opamp is a two stage amplifier followed by an emitter-follower buffer, and it is biased with an on-chip current source. The die photo is shown in Figure 56, showing the location of each circuit on the chip. The output voltage of the regulator is given by

$$Vout = Vref(1 + \frac{R_7}{R_8}). \tag{25}$$

The SiGe BGR circuit is designed to generate an output voltage of 1.17 V at room temperature, and an output voltage of 1.65 V is expected from the regulator. During normal circuit operation, the substrate is grounded, and a power supply of 3.3 V is used to bias the circuit.

The regulator circuit, along with transistor test structures consisting of 4 parallel HBTs with emitter area of 0.5×2.5 μm^2, were mounted onto a high-speed board (Figure 57) which was specifically designed for this experiment. Using 1 mil gold bond wires, each terminal of the device under the test, was wirebonded to an on-board transmission line with impedance characteristic of approximately 50 Ω. 18 GHz subminiature version A (SMA) connectors were provided at the back of the board for each terminal to establish electrical connectivity. These SMA launchers were connected to the terminals of a Tektronix DPO72004 20 GHz (50 GS/s) real-time digital oscilloscope via 40 GHz cables and through 40 GHz bias tees. Note that

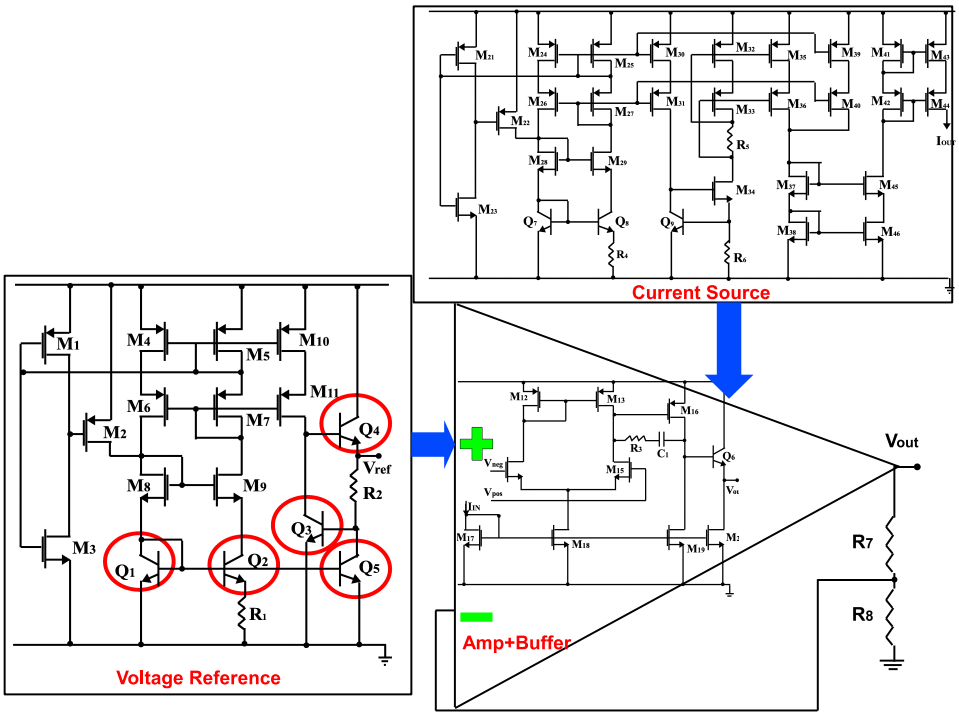

Figure 55: Schematic of SiGe voltage regulator.

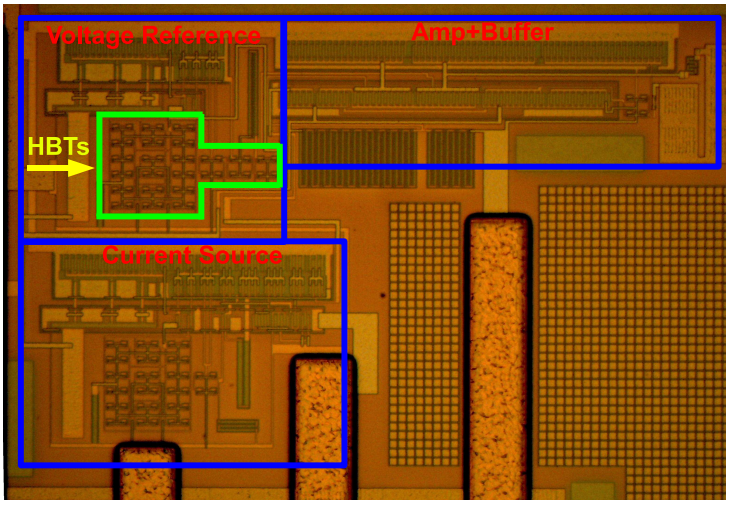

Figure 56: Die photo of the SiGe voltage regulator.

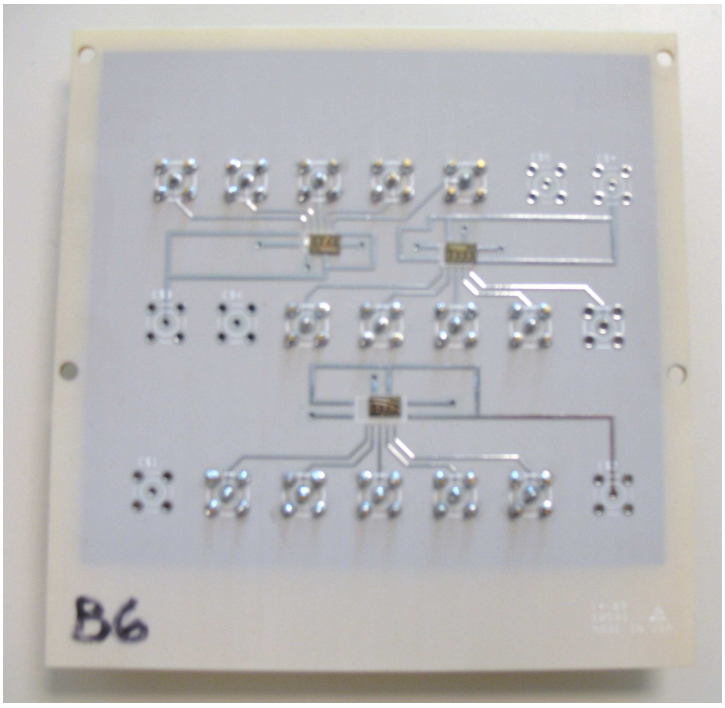

Figure 57: High-speed board for capturing transients.

the DC voltage was blocked by the capacitor inside the bias tee and therefore, the transients have been captured on the scope with 0 DC offset.

TRIBICC testing was performed at Sandia National Laboratory using 36 MeV ^{16}O ions, with a peak LET of 5.4 MeV.cm^2/mg. During ion strike, the regulator circuit was maintained under normal operating conditions, and all terminals of the transistors were grounded except for the substrate, which was biased at -4 V.

7.2 Results and Discussions

The HBT structures, consisting of 4 0.5×2.5 μm^2 transistors, were bombarded by oxygen ions, and the corresponding transient currents at all four terminals were captured. Figure 58 shows the location of the strikes that have generated transient events while scanning the beam over the area of the four transistors. As expected, no transients was collected for strikes outside the HBT's deep trench. Note that blue

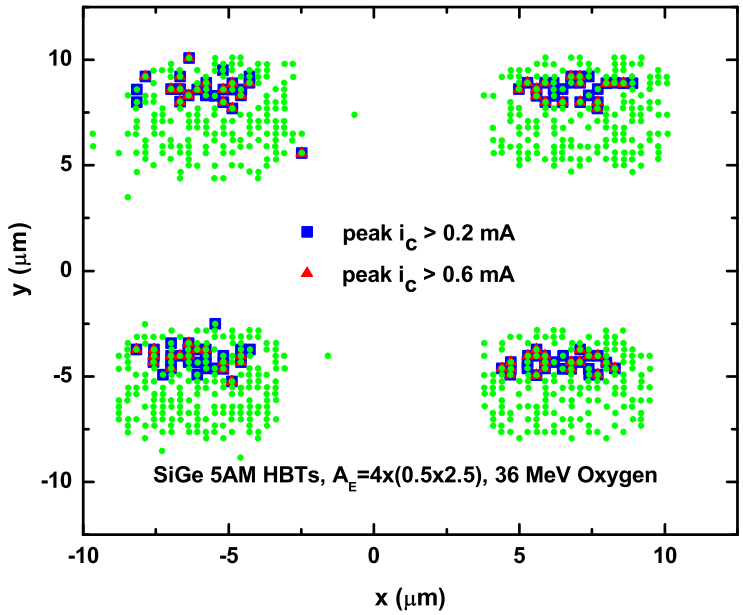

Figure 58: Map showing the locations of occurred transients for 4 parallel SiGe HBTs.

squares in Figure 58 correspond to the locations of strikes causing transient currents at the collector terminal with magnitude larger than 0.2 mA. It can be seen that the magnitude of transient currents for strikes over the emitter is significantly larger than the magnitude of transients for strikes outside the emitter (as expected). The base and collector transient waveforms for strikes outside and over the emitter area of HBTs are plotted in Figures 59 and 60, respectively. The transient currents exhibit the classical exponential shape with fast rise times followed by a larger fall time. In both figures, the duration of the transient currents appear to be less than 1 ns.

The SiGe HBT bank in the BGR circuit (transistors Q_1-Q_5 in Figure 55, also highlighted in Figure 56), was targeted for heavy ion strikes. Note that transistors Q_1, Q_3-$Q5$, each, consists of four parallel 0.5×2.5 μm^2 transistors. Transistor Q_2 consists of 32 parallel 0.5×2.5 μm^2 SiGe HBTs. To achieve better matching between Q_1 and Q_2, a common centroid layout technique was employed (32 transistors of Q_2

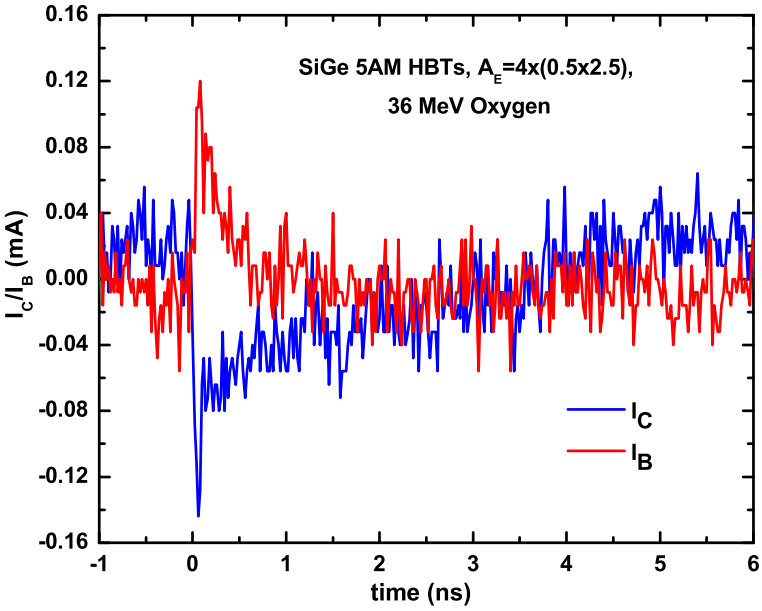

Figure 59: Base and collector current transients for strikes outside the emitter.

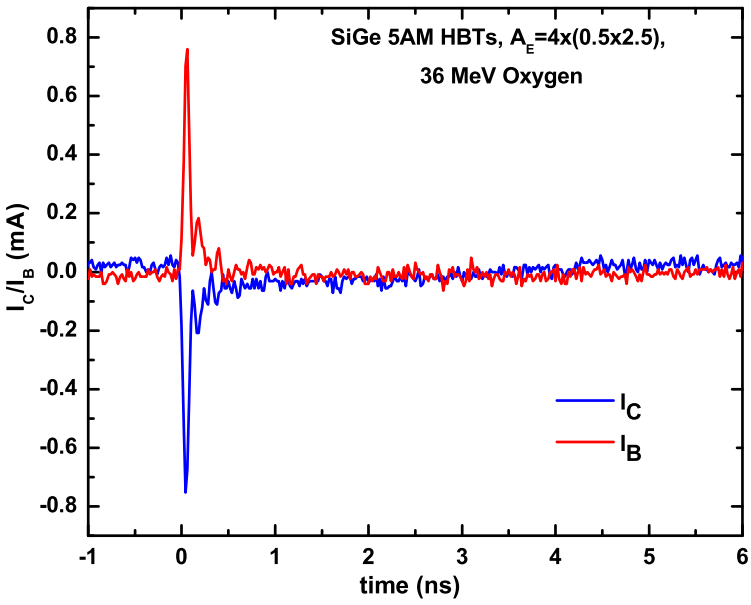

Figure 60: Base and collector current transients for strikes over the emitter.

surround Q_1).

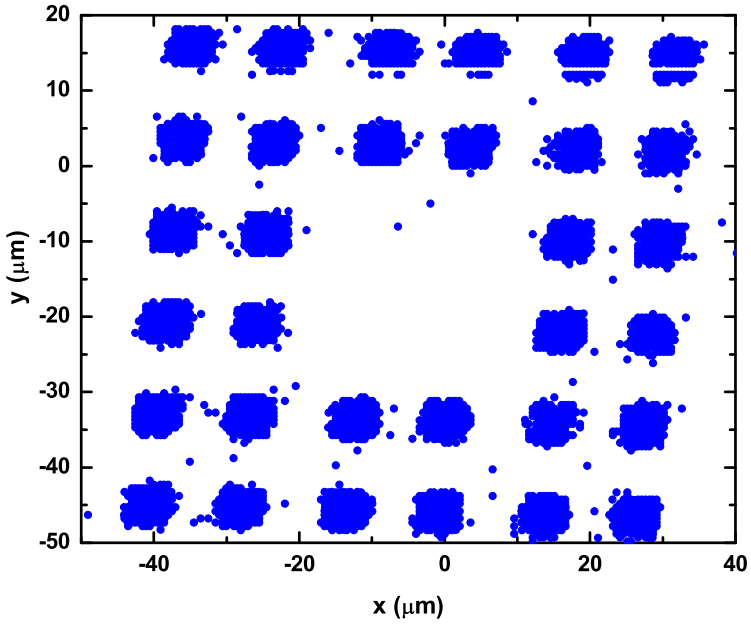

Figure 61: Map showing the locations of occurred transients for the HBT band in SiGe BGR.

As the beam is scanned over the HBT block, transients at the output of the regulator were captured. The transient waveforms in the output voltage of the regulator for the most common events are shown in Figure 62. Depending on the location of the strike, the magnitude and the duration of the transients vary from one event to another. The map showing the location of captured events, when striking Q_1 and Q_2, is shown in Figure 61. It was observed that transient response strongly depends on the location of the ion strike. Interestingly, transistors Q_1 and Q_3 are shown to be insensitive with respect to SET. Emitter strikes on transistor Q_4, creates transients with small peak magnitude, and the mirroring transistors, Q_2 and Q_5 are responsible for generating large transients.

Comparing Figure 62 with Figure 60 shows that transients at the output of the regulator have significantly longer duration and magnitude than the transients captured

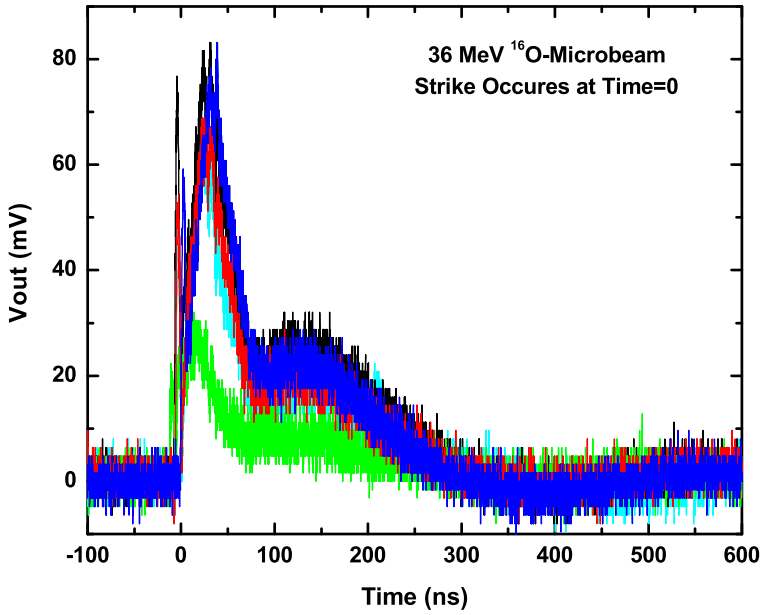

Figure 62: Measured transient response of the SiGe voltage regulator.

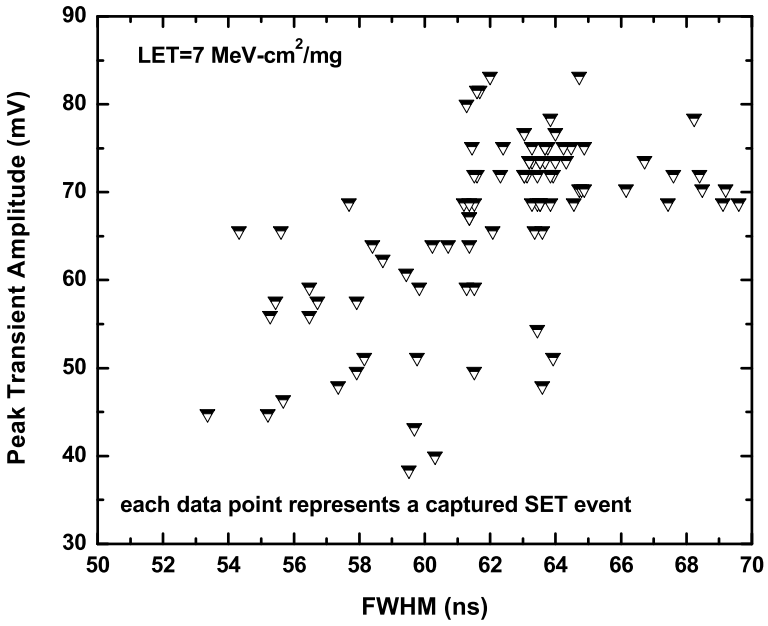

Figure 63: Measured SET event peak magnitude as a function of FWHM.

at the transistor level. This is due to the fact that the load and biasing condition of the transistor, when used in the circuit, and when it is tested as a singular device, are not the same, and therefore, the SET response under the two conditions are expected to be different.

The peak transient magnitude, as a function of full-width-half-maximum (FWHM) pulse width, for the most common events, is shown in Figure 63. This plot indicates that the largest observed peak magnitude for ^{16}O ion-induced transients of the regulator is less than 84 mV. Figure 63 can be used as the preliminary evaluation of SiGe regulator's SET response to determine if the circuit can be safely used for a specific application.

7.3 Summary

In this chapter, we studied the SET response of a SiGe BGR circuit through heavy ion microbeam experiment. The BGR was used in a regulator configuration. The SiGe HBTs inside the BGR circuit were struck by 36 MeV ^{16}O ions and the corresponding transients were captured at the output of the regulator. It was shown that depending on the location of the strike, the magnitude and the duration of the transients vary from one event to another. Sensitive transistors, responsible for creating large and long transients, were identified in the BGR circuit.

CHAPTER VIII

THE IMPACT OF PROTON IRRADIATION ON HIGH-VOLTAGE TRANSISTORS

Unmanned robotic space missions require high-voltage (HV) transistors (e.g., 20 V) for use in motor actuators and input/output interface circuits. In order to have a low cost and fully integrated system-on-a-chip for space missions, it is desirable to have these HV transistors fabricated on the same substrate as the low-voltage (LV) SiGe HBTs and MOSFETs (e.g., 3.3 V). The integration of HV transistors within existing LV processes has been a topic of significant interest for decades [126]- [131]. In general, HV operation in a standard process is achieved by using either circuit or device techniques [127]. Circuit techniques usually involve cascading LV transistors to effectively achieve HV operation. This approach, however, increases the circuit complexity and the required power to maintain intermediate voltages for gate drive [131]. Among the proposed device techniques, lateral double-diffused MOS (LDMOS) and drain-extended MOS (DEMOS) structures are the most popular solutions for fabricating HV transistors on the same substrate as LV transistors. LDMOS devices require extra masks and processing steps [128], while DEMOS transistors are relatively easy to fabricate, since they share the same uniformly doped channel with their LV counterparts [129]. Before these HV devices can be used on long term space missions, however, their performance under extreme environment conditions (over wide temperature range and under radiation exposure) needs to be thoroughly evaluated. In addition, the operative damage mechanisms involved in causing possible performance degradation under such extreme conditions must be understood. In terms of radiation response of HV transistors, only a few studies have been conducted [33],

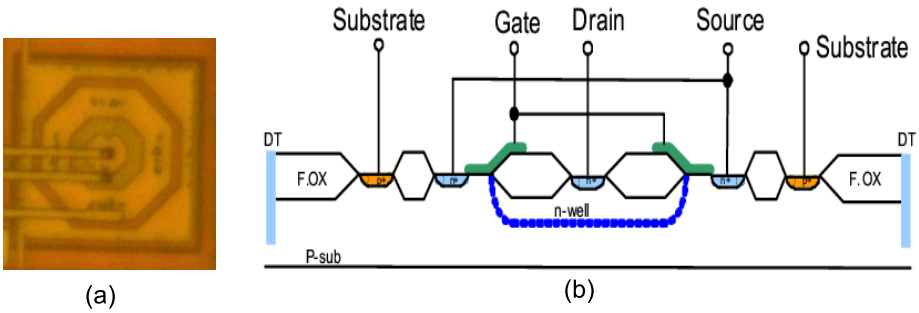

Figure 64: (a) Layout and (b) cross-section of a HV nMOS transistor implemented in first-generation SiGe BiCMOS platform.

[132], [133]. The work in [132] and [133] focused on the radiation response of LDMOS transistors implemented in SOI and SIMOX platforms, respectively, while in [33] the preliminary response of a prototype HV transistor implemented in a SiGe technology is briefly discussed.

In this chapter, we present a comprehensive investigation of the impact of proton irradiation on the performance of HV transistors implemented in a first-generation 3.3 V SiGe technology. HV transistors are irradiated under several different biasing conditions. Experimental results are presented and discussed. Differences in the radiation response of the HV and LV transistors are highlighted. These differences suggest that the degradation mechanisms involved in LV and HV transistors could be of fundamentally different origins and thus motivates further in-depth investigation.

8.1 HV Devices in SiGe Technology

For this study, HV transistors were implemented in a first-generation 3.3 V SiGe BiCMOS technology (IBM's SiGe 5AM) platform by employing special layout techniques. No process changes were made to the technology and no additional mask layers were

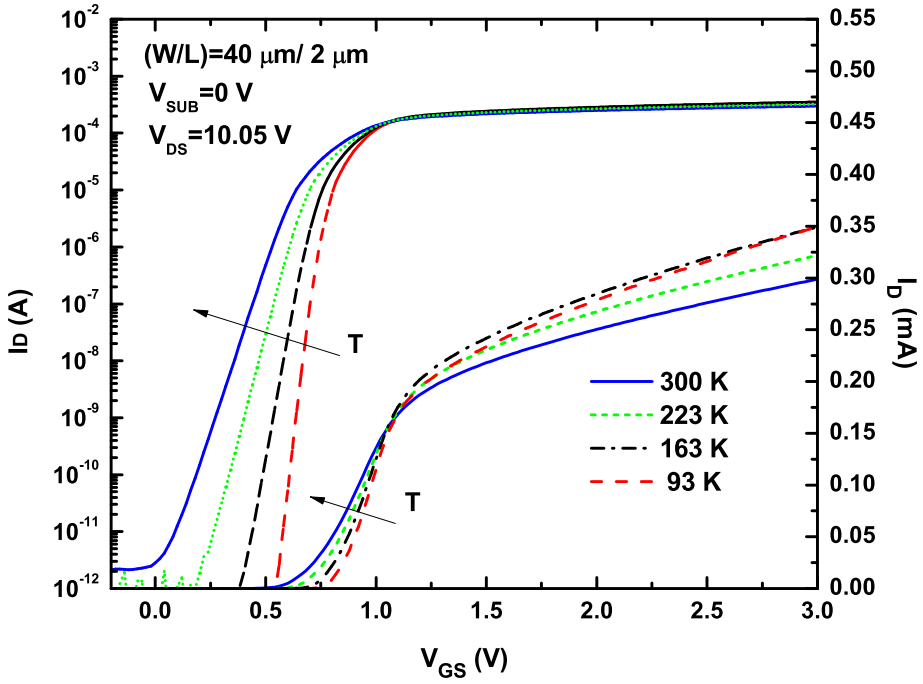

Figure 65: I_D-V_{GS} characteristics of a HV nMOS transistor as a function of temperature.

utilized. Avalanche breakdown located at the edge of the drain is the primary factor in limiting the voltage blocking capability of the conventional nMOS transistors [129]. To build HV transistors compatible with standard LV transistors new device structures must therefore be created. Layout and cross-section of such a HV transistor is shown in Figure 64. This device is based upon a conventional n-channel MOSFET with the drain area surrounded by an n-well. The n-well is used to define the lightly doped n-type "drift" region [129]. Since the n-well has a low surface doping level, the surface electric field is decreased, resulting in a device with a high breakdown voltage. Three independent layout parameters; namely, the channel length, the gate overlap of the drift region, and the length of the lightly doped drift region, can influence the performance, the breakdown voltage, and the reliability lifetime characteristics of this HV transistor, and thus need to be carefully addressed [134]. The transistors chosen

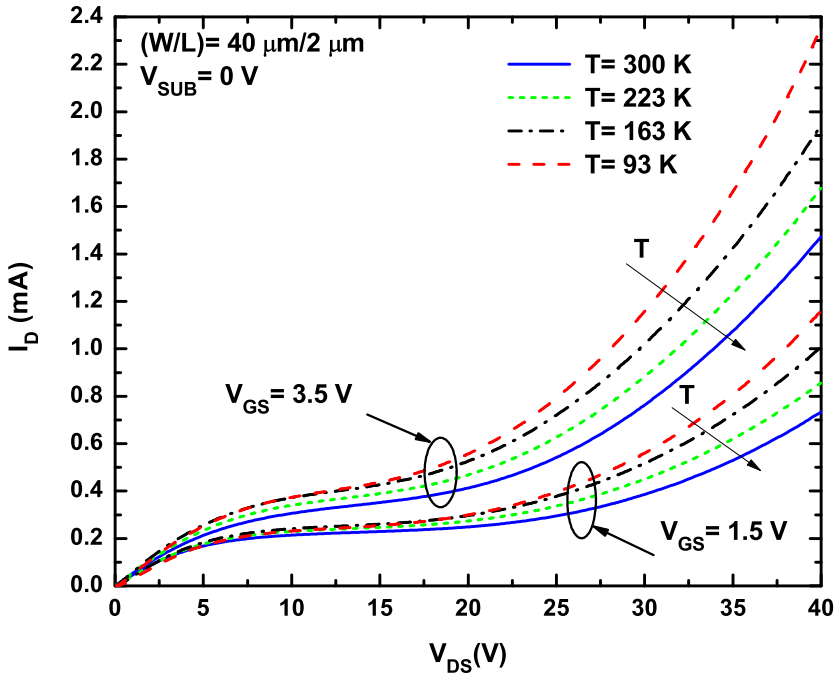

Figure 66: I_D-V_{DS} characteristics of a HV nMOS transistor as a function of temperature.

for this study have a gate length of 2 μm and gate width of 40 μm. With the drift region length of 4.35 μm, a blocking voltage of 57 V was achieved, which is more than adequate for the intended application.

8.2 Experiment

63 MeV proton irradiation was performed at the Crocker Nuclear Laboratory at the University of California at Davis, at a dose rate of 1 krad(Si)/s. A total number of 14 HV transistors with (W/L) =40$\mu m/2\mu m$ from two fabrication experiments were mounted in 28-pin DIP ceramic packages, wire bonded, and extensively characterized before being irradiated. Since these devices were designed by manipulating their layout and intentionally violating selected design rules, variations among different transistor designs are expected. Irradiation was performed at room temperature and

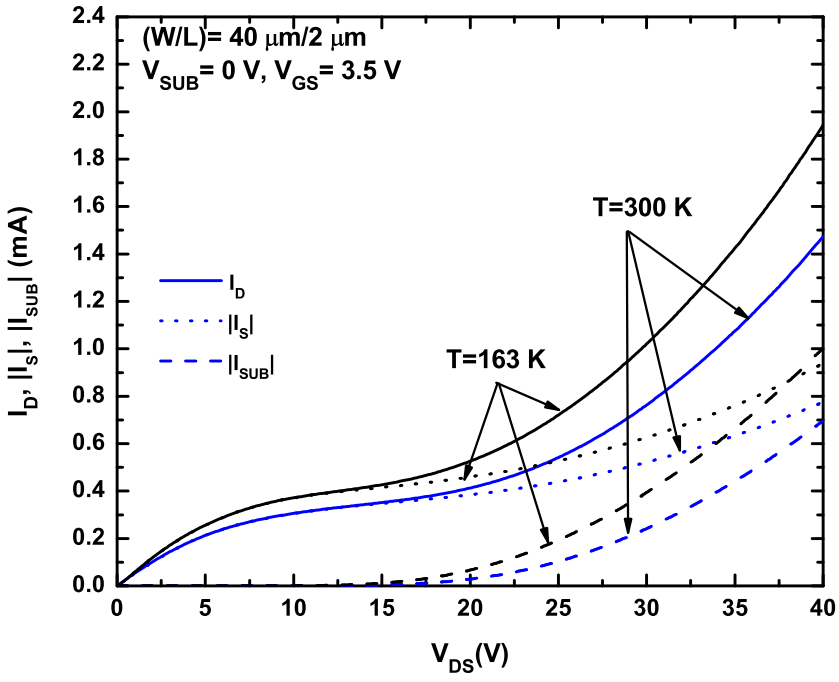

Figure 67: I_D, $|I_S|$, and $|I_{SUB}|$ as a function of V_{DS} for a HV nMOS transistor at two temperatures.

under different biasing conditions. At least two samples were considered for each irradiation experiment. Post-irradiation measurements were performed two weeks after irradiation. Experiments and measurement results are discussed in the following sections.

8.3 Results and Discussion

Figure 65 shows the subthreshold characteristics of a HV nMOS transistor with W/L=40μm/2μm, measured at V_{DS}=10.05 V and at four different temperatures. Similar to LV nMOS transistors, the subthreshold slope and the threshold voltage increase and the subthreshold leakage decreases as the temperature is reduced. The transistor exhibits a zero temperature coefficient bias point in the vicinity of the gate-source voltage of 1.1 V. The output characteristics of the same HV transistor

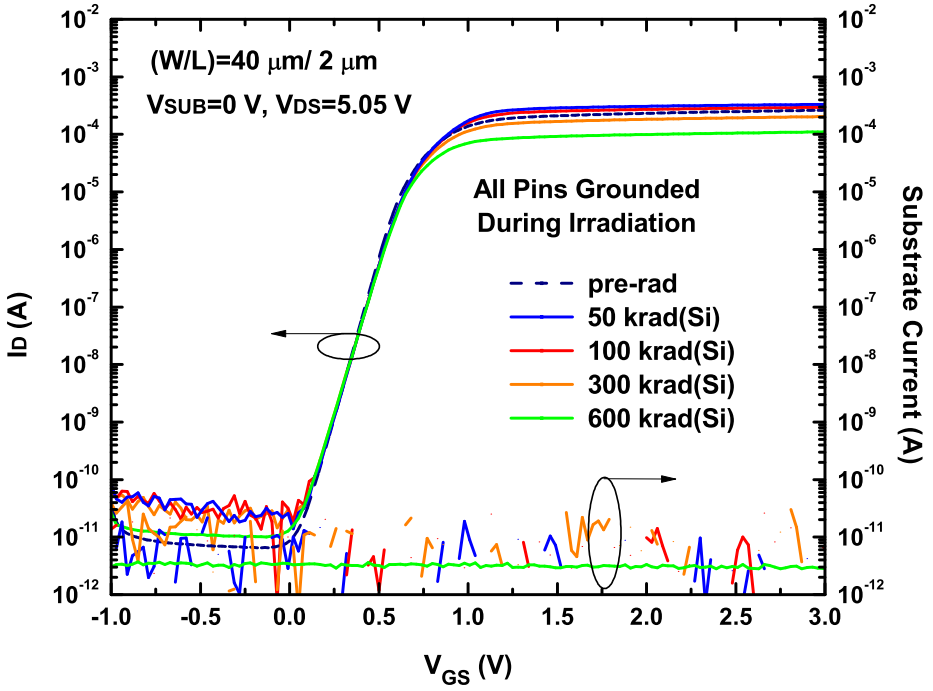

Figure 68: I_D-V_{GS} and I_{SUB}-V_{GS} characteristics of a HV nMOS transistor as a function of dose for irradiation with all pins grounded.

measured at two gate-source voltages and at four different temperatures are shown in Figure 66. The drain current and the output conductance in the saturation region increase as the temperature decreases, similar to what is expected from LV nMOS transistors [135]. Observe that, at a certain temperature, the output conductance is negligible for V_{DS} <20 V but increases beyond V_{DS}=20 V. To gain more insight into this, the drain current and the absolute values of the source and the substrate currents at two temperatures are plotted in Figure 67. As can be seen, the substrate current starts to increase for V_{DS} >20 V (onset of impact ionization). The increase in the output conductance at high drain voltages has been also observed in HV transistors fabricated in technologies other than SiGe technology [127], [131].

Figures 65 and 66 verify that these HV transistors can reliably function in the

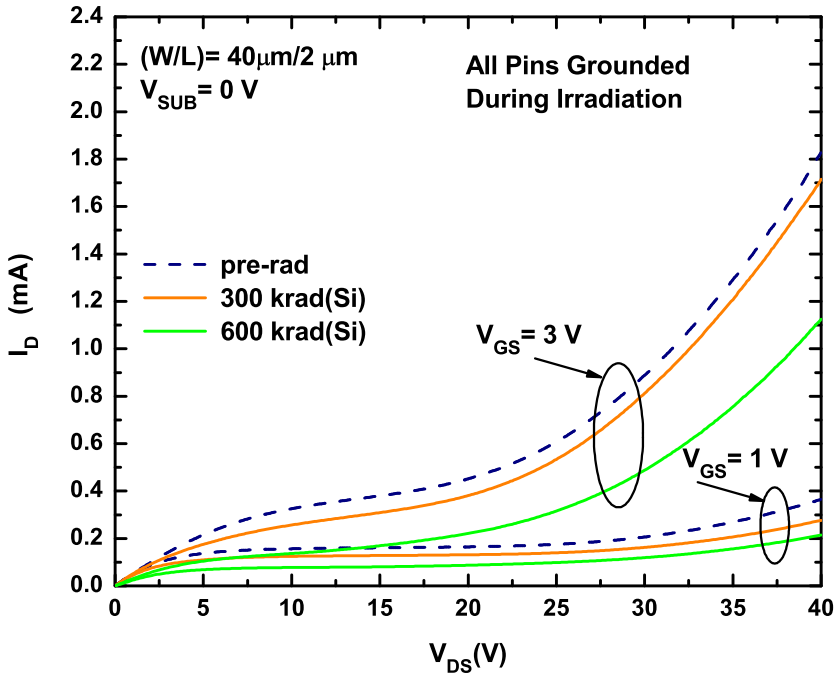

Figure 69: I_D-V_{DS} characteristics of a HV nMOS transistor as a function of dose for irradiation with all pins grounded.

range of $V_{DS} < 20$ V to temperatures as low as 93 K, the intended application in this case. To ensure the extreme environment capability of these transistors, in addition to their cryogenic performance, their radiation response needs to be thoroughly studied. Proton irradiation was performed under three different biasing conditions: 1) irradiation with all pins grounded, 2) irradiation under gate bias, and 3) irradiation with biased gate and substrate. The impact of operating substrate bias was also investigated. The following sections present the experimental results from each radiation experiment.

8.3.1 Irradiation with All Pins Grounded

Figure 68 depicts the I_D-V_{GS} characteristics for a HV transistor irradiated with all pins grounded, as a function of equivalent total dose. The characteristics were measured

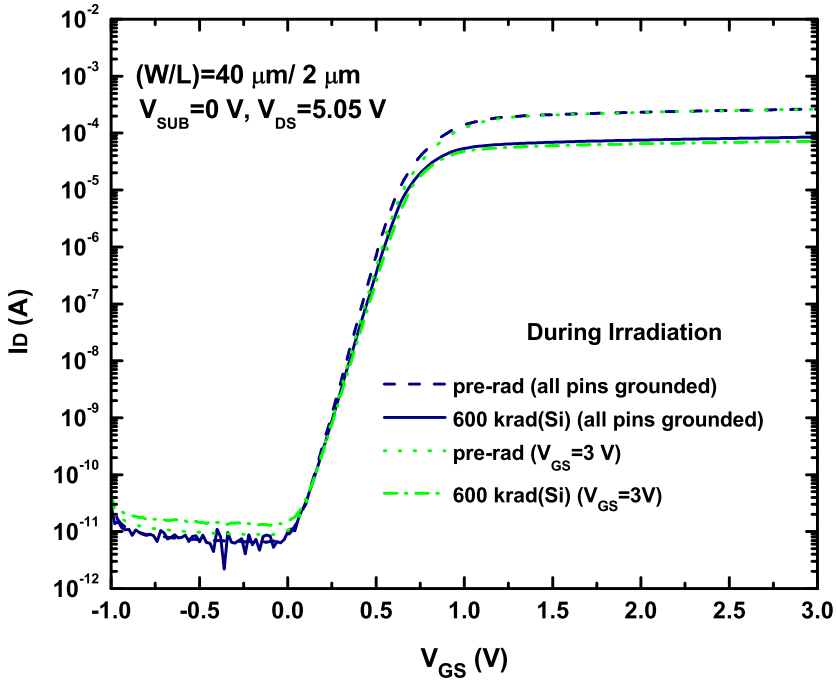

Figure 70: I_D-V_{GS} characteristics of HV nMOS transistors for V_{GS}=3 V and 0 V irradiation conditions.

at V_{SUB}=0 V and V_{DS}=5.05 V. The degradation in the threshold voltage is negligible after irradiation, as expected. Similar to LV NMOS transistors, the off-state leakage increases after irradiation. Interestingly, however, the increase in the leakage current remains below 100 pA, even after exposure to total ionization dose level of 600 krad(Si). It was observed that the leakage current in LV NMOS transistors in this SiGe technology increases to about 10 μA after irradiation to TID level of only 100 krad(Si) [58]. In LV NMOS transistors, typically two radiation-induced leakage mechanisms are responsible for causing the subthreshold leakage current. One mechanism, known as Gate-Induced-Drain-Leakage (GIDL), is the radiation-induced tunneling (band-to-band and/or trap-assisted) in the gate-to-drain overlap region [136] which causes a negative slope in the drain current in V_{GS} <0 region. As the gate bias voltage is reduced, the junction field is increased, causing the minority carriers to

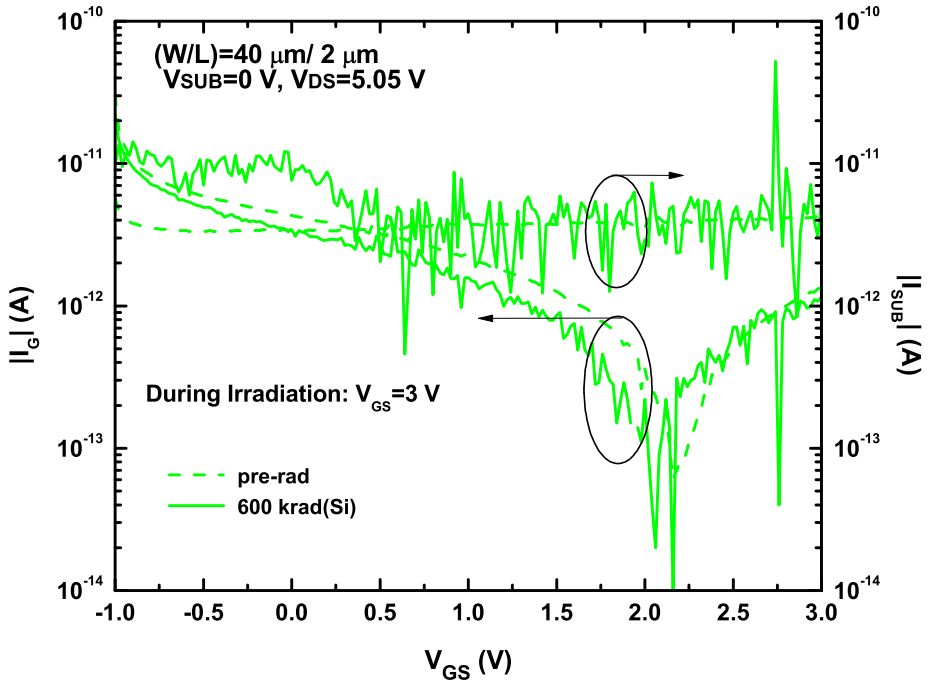

Figure 71: $|I_G|$, and $|I_{SUB}|$ characteristics of a HV nMOS transistors for V_{GS}=3 V irradiation condition.

be swept away into the substrate and resulting in an increase in the leakage current. The other cause of subthreshold leakage current is the presence of radiation-induced positive charges in the region where the gate extends over the shallow trench isolation (STI) edge, effectively creating a shunt leakage path from source-to-drain. This will result in a positive sloping drain current in the negative gate-source voltage region [137]. As seen from Figure 68, none of the two mentioned radiation-induced LV damage mechanisms are significantly involved in the operation of HV transistor, and the subthreshold leakage current does not increase substantially after irradiation. For a better understanding, the substrate current was also measured at each dose level and is plotted in the same figure. As can be seen, the substrate current level remains less than 10 pA after irradiation to total dose level of 600 krad(Si) and does not show any significant dependence on GIDL or STI edge leakage. The differences in the radiation

response of LV and HV transistors could be the result of differences in their layout structures. Further investigation is required to fully understand these differences and will be reported at a later date.

Figure 69 shows the I_D-V_{DS} characteristics of the same transistor measured at V_{SUB}=0 V and V_{GS}=1 V and V_{GS}=3 V. It is well known that the mobility of carriers is degraded as radiation dose is increased and as a result the current drive capability of the transistors is reduced [138]. It can be seen from Figure 69 that as soon as the transistor turns on, the drain current decreases after irradiation. The reduction in the drain current is more significant when the transistor is exposed to 600 krad(Si). This post-rad degradation can also be observed in the on-regime part of Figure 68. As discussed above, this degradation could be attributed to the decrease in the effective channel mobility after radiation. Similar post-rad current drive capability degradation was observed in power MOSFETs [139].

8.3.2 Impact of Irradiation Gate Bias

It is well known that gate bias during irradiation significantly increases the leakage current in LV nMOS transistors [140]. To investigate the impact of irradiation gate bias on the DC performance of HV nMOS transistors, HV transistors were irradiated at the gate bias of 3 V to total equivalent dose level of 600 krad(Si). The substrate voltage was set to ground during the irradiation. I_D-V_{GS} characteristics were measured for V_{DS}=5.05 V and the results are plotted in Figure 70. Measurement results from grounded irradiation experiment are also included for ease of comparison. The figure shows that the increase in the subthreshold leakage current for V_{GS}=3 V irradiation is slightly higher than for V_{GS}=0 V irradiation. However, the leakage remains below 100 pA, which is acceptable for circuit operation, without employing any radiation hardening techniques. In order to gain more insight for the involved degradation mechanisms, the absolute values of the substrate and gate currents are

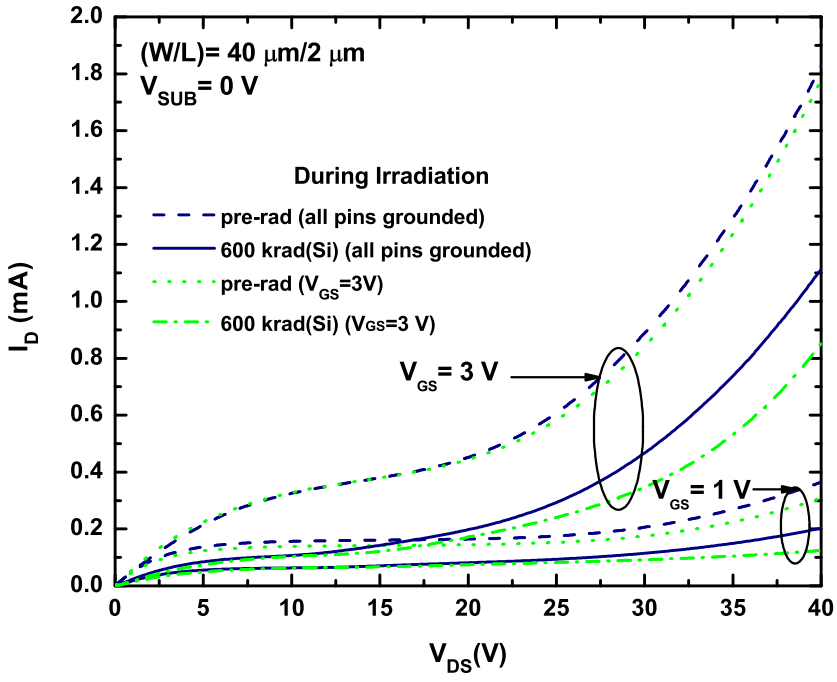

Figure 72: I_D-V_{DS} characteristics of HV nMOS transistors for V_{GS}=3 V and 0 V irradiation conditions.

plotted as a function of V_{GS} in Figure 71. As can be seen, there is negligible change in the gate current after irradiation. However, the substrate current increases after irradiation under gate bias (as expected) and this the cause of the slight increase in the subthreshold leakage current.

Figure 72 shows the I_D-V_{DS} characteristics of two HV transistors, one irradiated with all pins grounded and one irradiated under applied gate bias, measured at 0 V operating substrate and V_{GS}=1 V and V_{GS}=3 V. It can be seen that the drain current decreases after irradiation. This degradation is more significant at V_{GS}=3 V for the gate-bias irradiation. This degradation in the current drive capability, again, can be attributed to the degradation in the effective channel mobility.

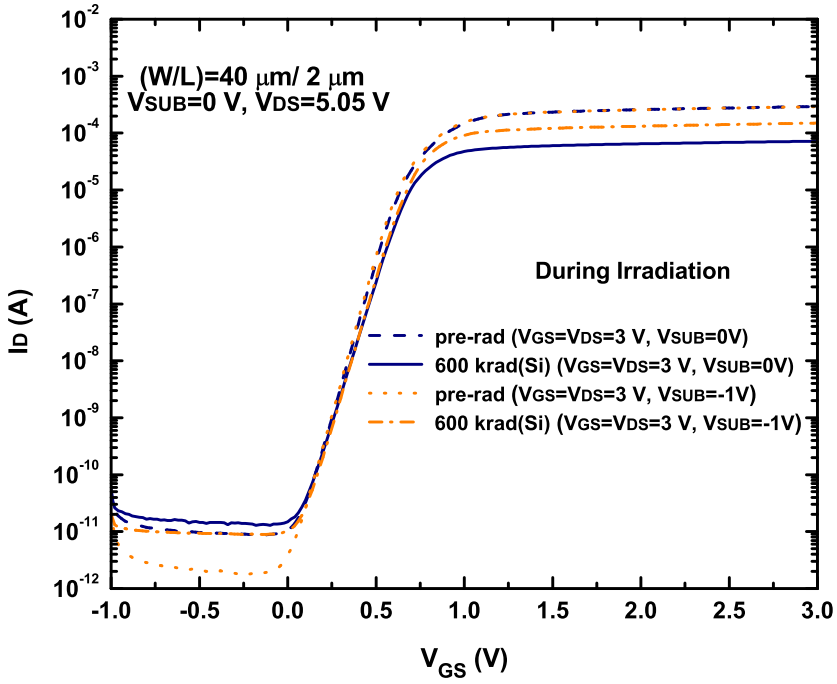

Figure 73: I_D-V_{GS} characteristics of HV nMOS transistors for irradiation substrate bias of 0V and -1 V.

8.3.3 Impact of Substrate Bias During Irradiation

To investigate the impact of substrate bias during irradiation, HV transistors were irradiated under V_{GS}=V_{DS}=3 V and with 0 V and -1 V substrate bias conditions. Figure 73 illustrates I_D-V_{GS} characteristics from this experiment measured at 0 V substrate voltage and V_{DS}=5.05 V. Observe that the increase in the leakage current is higher for the transistor irradiated at -1 V substrate voltage than for the one irradiated at 0 V substrate voltage. The increase in the subthreshold leakage after irradiating the transistor under negative substrate voltage is consistent with what has been observed in LV NMOS transistors [137]. However, the level of radiation-induced leakage current in these HV transistors is significantly smaller than that of LV transistors as the leakage current remains below 100 pA. The absolute values of the substrate and gate currents are plotted in Figure 74 as a function of gate-source

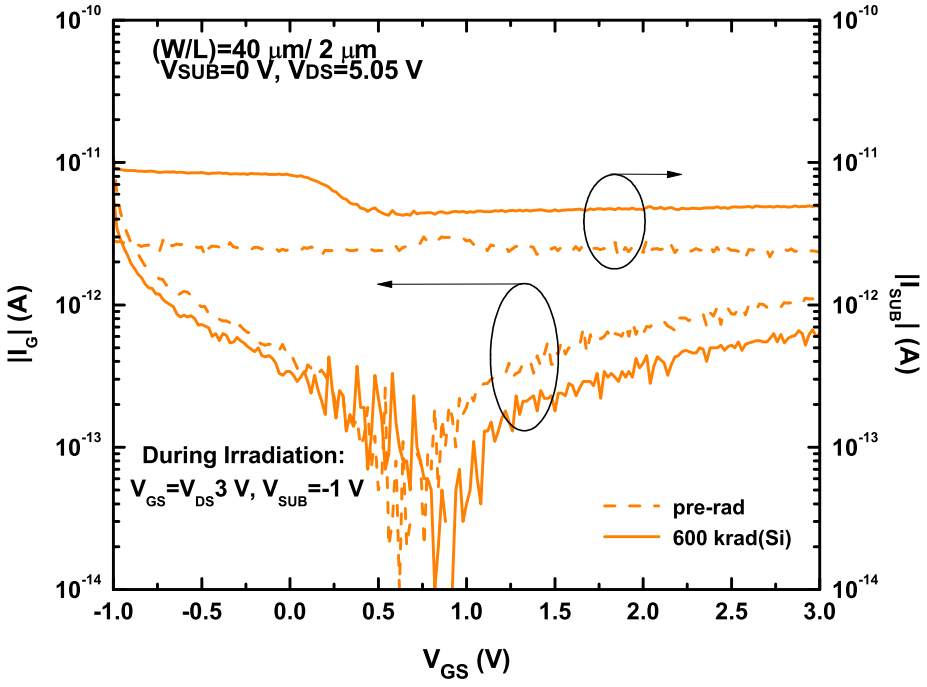

Figure 74: $|I_G|$, and $|I_{SUB}|$ characteristics of a HV nMOS transistors for V_{GS}=V_{DS}=3 V and V_{SUB}=-1 V irradiation condition.

voltage. Slight increase in the substrate current is observed after irradiation, which results in an increase in the subthreshold leakage current. The gate current slightly decreases after irradiation.

I_D-V_{DS} characteristics of HV transistors irradiated under substrate voltages of 0 V and -1 V are shown in Figure 75. Output characteristics are measured at V_{GS}=1 V and V_{GS}=3 V. As can be seen, the current drive capability has been less degraded after irradiation with negative substrate bias.

8.3.4 Impact of Substrate Bias Post Irradiation

It is has been previously shown that negative operating substrate bias can suppress the radiation-induced STI subthreshold leakage in LV nMOS transistors [137]-[140]. To examine the effects of negative substrate bias operation on the performance of HV nMOS transistors, I_D-V_{GS} characteristics of a transistor irradiated under V_{GS}=V_{DS}=3

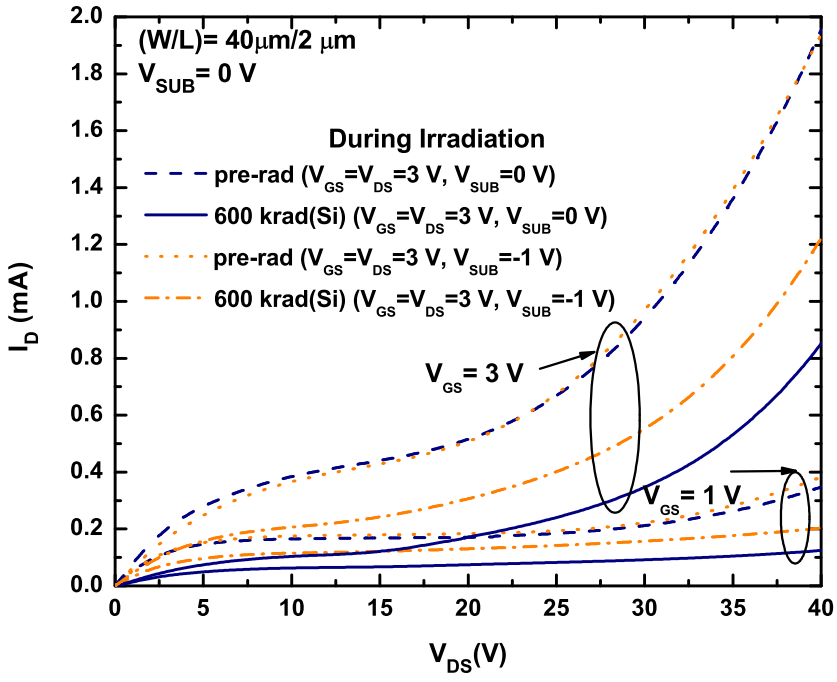

Figure 75: I_D-V_{DS} characteristics of HV nMOS transistors for irradiation substrate bias of 0V and -1 V.

V and V_{SUB}=-1 V were measured at a substrate potential of both 0 V and -1 V. Measurement results are plotted in Figure 76. Contrary to what is expected in LV transistors, no significant improvement was observed in the post-radiated subthreshold leakage current of HV transistors when a negative voltage is applied to the substrate.

8.4 Summary

In this chapter, we presented experimental results of the effects of proton irradiation on the performance of high-voltage (HV) nMOS transistors implemented in a low-voltage (LV) SiGe BiCMOS technology. The impacts of irradiation gate bias, irradiation substrate bias, and operating substrate bias on the radiation tolerance of these transistors were investigated. It was shown that the radiation-induced subthreshold leakage current of these HV transistors under different irradiation biasing

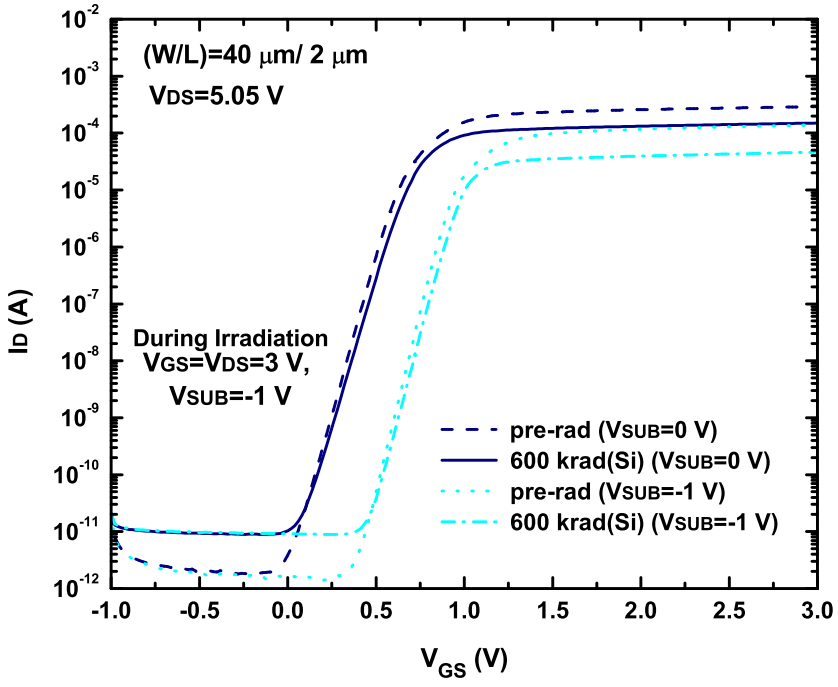

Figure 76: Comparison of I_D-V_{GS} characteristics of a HV nMOS transistor for operating substrate bias of 0 V and -1 V. The irradiation bias conditions were V_{GS}=V_{GD}=3 V and V_{SUB}=-1 V.

conditions, remains below 100 pA to 600 krad, clearly good news for circuits required for unmanned space missions. It was observed that the level of radiation-induced leakage current in the HV transistors is significantly smaller than that of LV transistors. A careful comparison of the radiation response of HV transistors and their LV counterparts reveals some significant differences. This suggests that the mechanisms involved in causing degradation in LV and HV transistors could be of fundamentally different origins.

CHAPTER IX

EXTREME ENVIRONMENT OPERATION OF DATA CONVERTERS

Data converters provide the means of interfacing digital systems with the analog world. In many applications, the architecture and the performance of the entire system are dependent on the ADC's capability. These applications for instance include military radar system [141], sampling oscilloscopes [142], high speed soft-decision-based forward error correction systems [143], and satellite and wireless communications [144], [145].

ADCs can also be very useful in space applications where detectors and cryogenic readout electronics are widely used. Currently, the analog output signal from these electronics is transported to warm boxes, where the ADC and other digital signal processing electronics exist. Having a cryogenic ADC which converts the analog signal to digital code before it is transported to a warm boxes, will greatly improve the signal integrity between cold and warm electronics [146]. However, ADCs capable of operating in harsh environments have not received sufficient attentions. Currently, the only available cryogenic ADCs are superconductive circuits [147] limited to operate to a maximum temperature of 10 K, and a 8-bit 3 kHz CMOS based ADC [146] which can operate at 4.2 K. In this chapter, we present the design procedure for a high-speed comparator and a flash ADC. Measurement results at room temperature for both the comparator and the ADC are presented. Predictions of how low temperature operation and irradiation damage will impact the performance of the comparator and the ADC are provided.

9.1 Platform For Extreme Environment Experiments

Figure 77 shows the chip micrograph of the platform designed to facilitate evaluating the extreme environment capabilities of data converters. This platform is designed to facilitate the extreme environment capability of key front-end building blocks of data converter implemented in SiGe technology. The circuits are implemented using third generation 210 GHz SiGe IBM's technology. The chip includes a high-speed comparator, a 3-bit current steering DAC, and a high-speed 3-bit ADC-DAC. The DAC output interface allows simple test evaluation of the ADC. The ADC employs flash architecture and the comparator circuit forms it's base unit. Without bondpads, the comparator, the DAC, and the ADC-DAC circuits occupy an area of 70 $\times$ 170 μm^2, 77 $\times$ 220 μm^2, and 200$\times$420 μm^2, respectively. The overall die size of the 3-bit quantizer-DAC circuit, including bondpads, is 1.76 $\times$ 1.27 mm^2. In what follows, we present the design and room temperature measurement results for the comparator and the ADC-DAC circuits.

9.2 Comparator

The comparator forms an essential building block of ADCs. The function of the comparator is to compare the input signal level with a reference point and consequently generate a logic output of "one" or "zero". The performance metrics of ADCs, including the maximum sampling rate, the bit resolution, and the total power consumption, are limited to the capabilities of their constituent comparator blocks. This is particularly true for the flash and two-step architectures. Monolithic high-speed comparators reported in the literature use a variety of technologies and architectures [148]-[154] and sampling rates up to 32Gs/s have been demonstrated [154]. Here, we present the design and room temperature measurement results for a 25 GS/s comparator implemented in the 0.12 μm SiGe technology. This comparator serves as the basic element of a 3-bit flash ADC, which will be discussed in the next section.

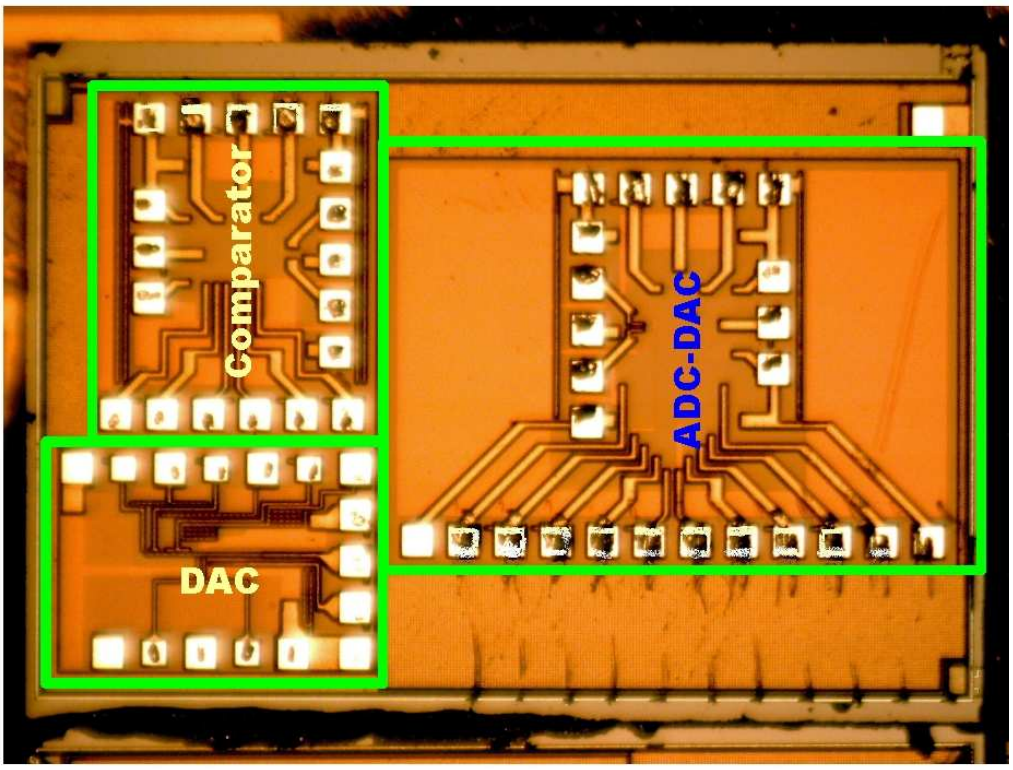

Figure 77: Platform for Extreme Environment Experiments.

9.2.1 Design

The block diagram of the comparator is shown in Figure 78. The comparator consists of a preamplifier, and two master/slave stages. The second master/slave stage was added to reduce the effective regeneration time constant [141].

The schematic of the preamplifier is shown in Figure 79. The differential pair amplifier with emitter followers at its input and output help to 1) reduce the kickback noise to acceptably low levels, 2)improve sensitivity to the small input voltage required to switch a comparators state by providing the high gain and thereby improving the resolution, and 3) lower the analog feedthrough from one input to the other [148], [154], [155]. The gain of the differential amplifier can be estimated as

$$A_v = \frac{2R_3}{gm_9^{-1} + gm_{10}^{-1} + 2R_2}, \tag{26}$$

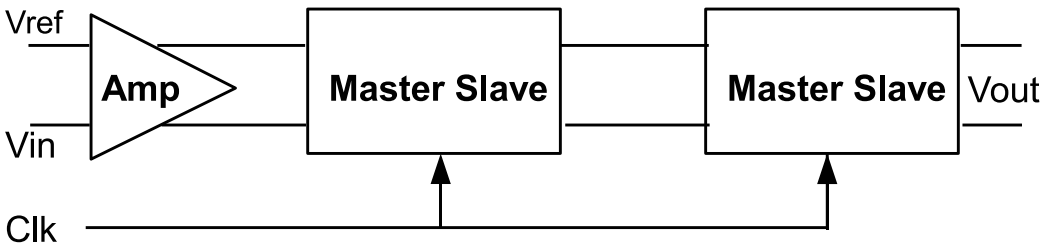

Figure 78: Block diagram of the high-speed comparator.

where gm_9 and gm_{10} are the transconductance of transistors Q_9 and Q_{10}, respectively. The emitter resistors were added to improve the linearity of the amplifier. Simulations show that with a power supply of 2.5 V and a tail current of 900 μA, the preamplifier provides 22 dB of differential gain and 8 GHz of -3 dB bandwidth.

The schematic of the master/slave latch is shown in Figure 80. Each latch consists of two cross-coupled differential pairs, current-switched in emitter-coupled logic (ECL) configuration. When the clock is high, the differential input is amplified by transistors Q_5 and Q_6 (in the master latch). Once the clock goes low, the input pair (Q_5 and Q_6) is disabled, and the second differential pair (Q_7 and Q_8) turns on to regeneratively amplify the differential output of the precedent stage, and to produce the corresponding logic levels. While the single latch can act as a comparator by itself, it will suffer from the problem of "metastability" , specially when the the input signal and the clock do not have timing relationship [155]. This problem arises when at the sampling instant, differential input voltage is close to the comparators minimum resolvable input. Since this initial input voltage can be considered as a random variable, the metastability can be expressed in terms of the probability of its occurrence as [156], [157]:

$$P(T > T_c) = \exp\left(\frac{-(A-1)T_c}{\tau}\right), \tag{27}$$

where T is the required regeneration time, T_c is the half of the clock cycle, and A and τ are the small signal gain and time constant of the each differential pair in the latch,

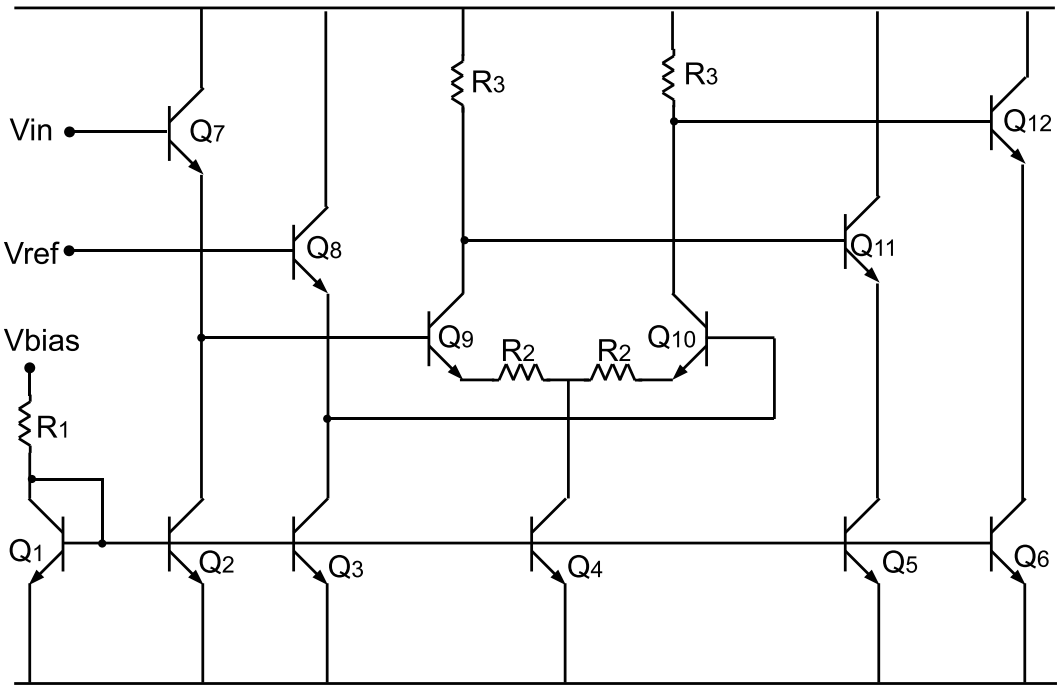

Figure 79: Schematic of the preamplifier.

respectively. Equation (27) shows that a larger gain or a shorter time constant for the differential pairs or pipelining the comparator output will reduce the probability of metastability [155]. In the design of the comparator, two master slave stages are used to effectively reduce the the probability of metastability. This ofcourse comes at the price of increase in chip's power and area. The emitter followers at the output of each latch provide a low output impedance for driving the following stage. In addition, they will improve both the regeneration speed and the bandwidth, by reducing the loading effect of parasitic capacitance of the their precedent differential pair stage [155].

The combination of the pre-amplifier and the flip-flop has a simulated minimum resolvable differential input of 800 μV at a clock frequency of 20 GHz with a power supply of 2.5 V. The minimum resolvable input signal increases as the clock frequency is increased. At a clock frequency of 33 GHz, the minimum resolvable signal is 5 mV.

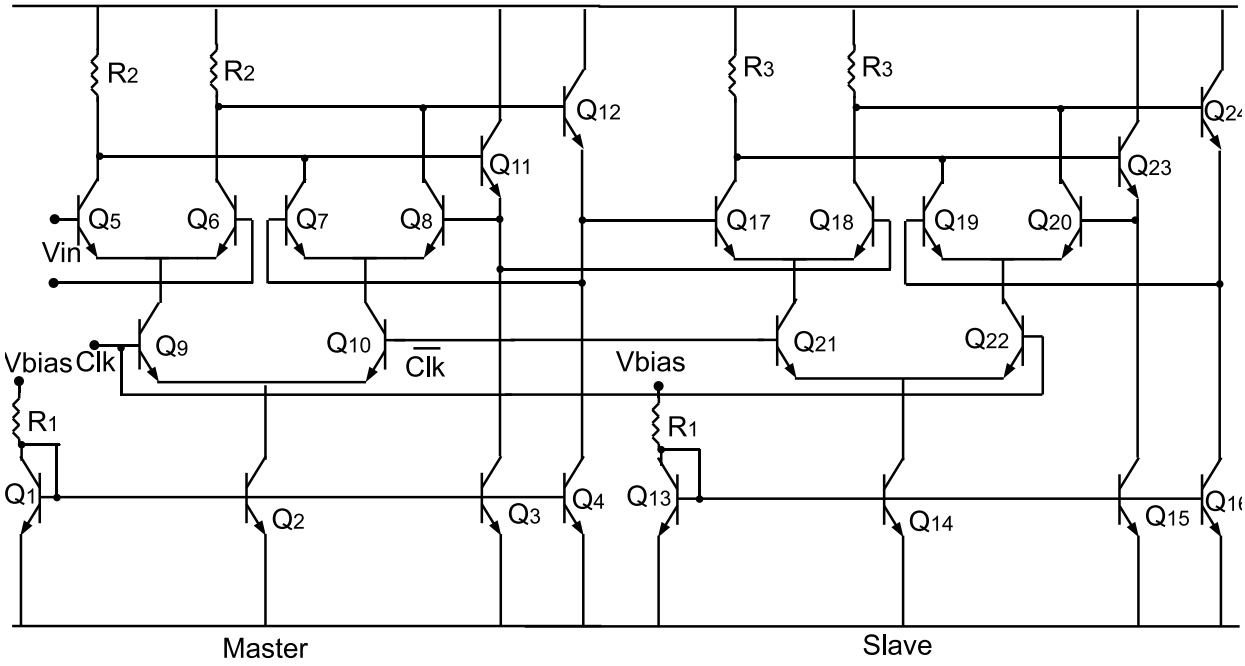

Figure 80: Schematic of the naster/slave block.

9.2.2 Measurement Results

On-wafer measurement was performed using 40 GHz probes and cables. Agilent 83640L continuous wave signal generator was used for the clock signal and a hybrid was used to convert the single-ended signal into a differential one. To ensure that the phase difference of the two complementary clock signals are properly maintained, phase tuners are used to adjust the phase of differential signals to exactly 180° after passing through the hybrid. A sinusoidal waveform with a DC level of 2 V was used as one input to the comparator. The second input to the comparator, $Vref$, was connected to a DC power supply. The output waveform was captured using a 12.5 GHz Tektronix 71254 digital phosphorous oscilloscope.

Figure 81 shows the measured output waveform of the comparator for a 3 GHz input signal clocked at 18 GHz for three different $Vref$ values. The amplitude of the input signal was kept constant during the three measurements. When the DC level of the sinusoidal signal is set to $Vref = 2$V (Figure 81-a), the high and low stages of

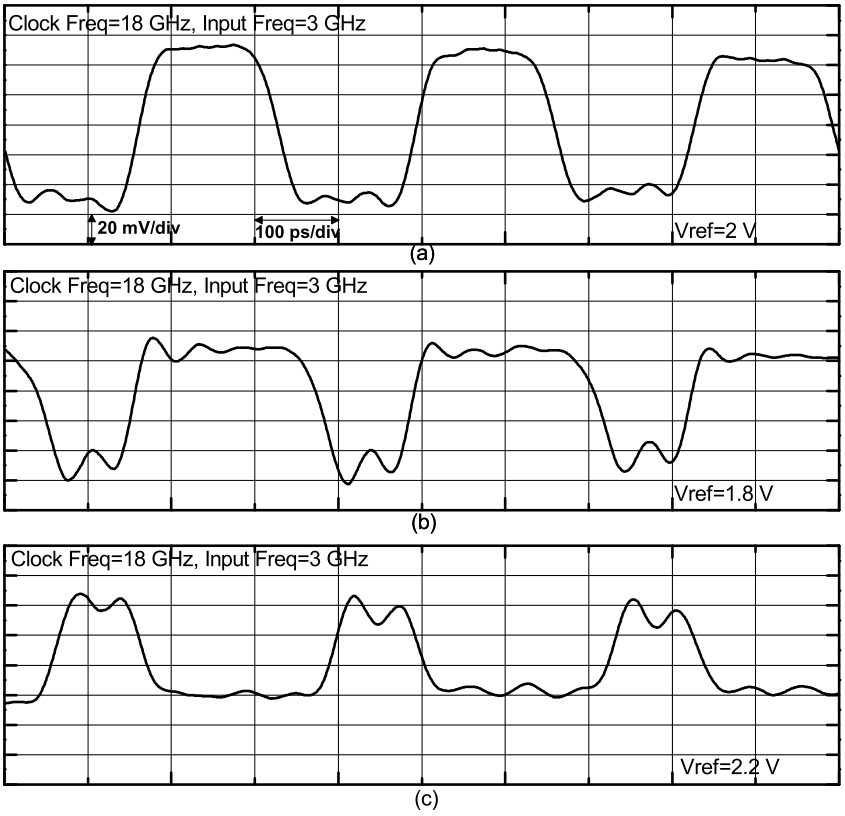

Figure 81: Measured output waveform of the comparator with 3 GHz input signal clocking at 18 GHz for three different input reference voltages; a) $Vref$=2 V, b)$Vref$=1.8 V, and c) $Vref$=2.2 V.

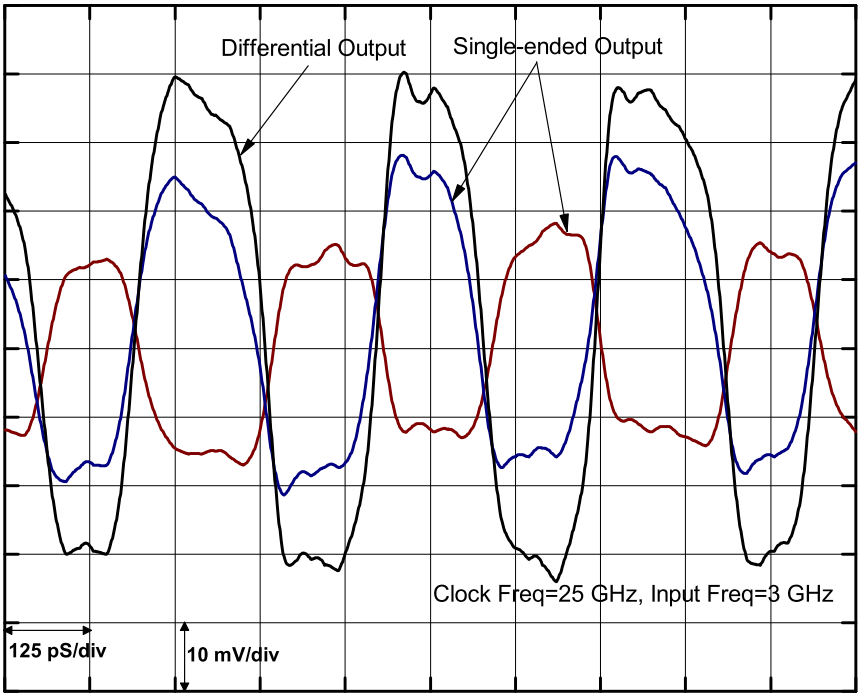

Figure 82: Measured output waveform of the comparator with 3 GHz input signal clocking at 25 GHz, Vref=2 V.

Table 7: Performance Summary and Comparison Table for high-speed Comparator

Reference	Sampling Rate (GHz)	Supply Voltage (V)	Power Dissipation (mW)	Technology Technology f_T (GHz)	Active Area (mm^2)
This Work	25	2.5	33	SiGe (210)	0.012
[154]	32	3.5	405	SiGe (200)	0.023
[148]	20	3.5	82	SiGe (120)	0.045
[149]	8	-6.0	N/A	GaAs (30)	N/A
[150]	16	N/A	221	SiGe (55)	0.096
[151]	5	3.0	89	SiGe (40)	0.058
[152]	4	1.8	2	0.18 μm CMOS	0.015
[153]	10	1.2	37	0.11 μm CMOS	0.007

the output waveform have equal widths. In Figure 81-a, the output waveform shows a measured rise/fall time (20% to 80%) of 24.12 ps and 29.65 ps, respectively. Changing the DC level of $Vref$ impacts the differential input voltage to the comparator. Comparing Figures 81-b and 81-c shows that decreasing the value of $Vref$ increases the high voltage pulse width, while increasing the value of $Vref$ increases the low voltage pulse width. At the clock frequency of 18 GHz, the frequency of the input signal was increased and the comparator showed reliable operation up to 8 GHz. The performance of the circuit, however, degrades for input frequencies larger than 5 GHz.

At the input frequency of 3 GHz, the clock frequency was raised to 25 GHz. Figure 82 shows the measured output waveform for the single ended and differential outputs with a rise/fall time of 43.37/43.17 ps. Operating with a 2.5 V power supply, the comparator dissipates a total power of 33 mW. Table 7 provides a performance summary and comparison to other high-speed stand-alone comparators. This high-speed comparator offers a low power consumption option with a comparable performance to [148]-[154].

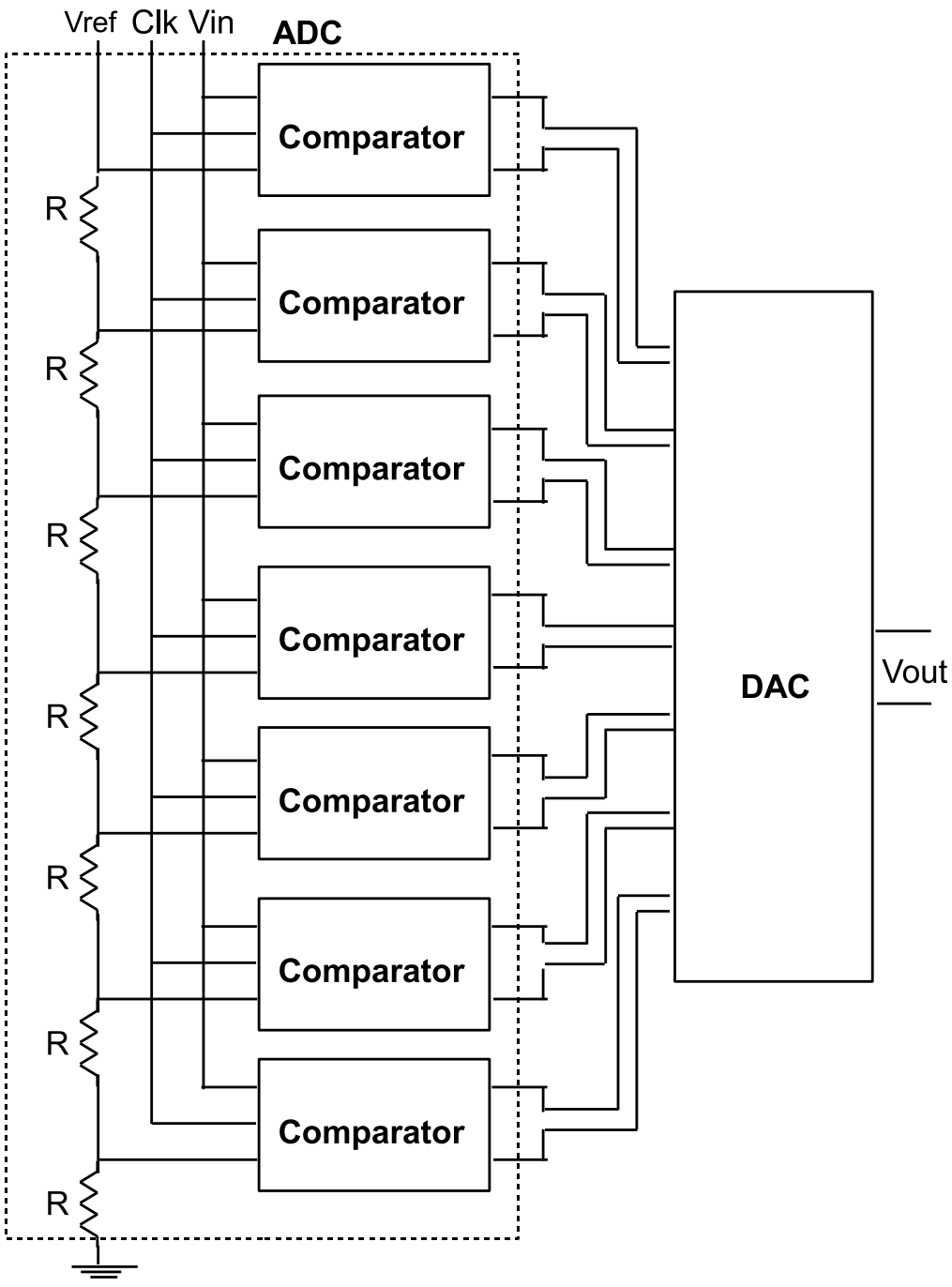

Figure 83: Block diagram of the 3-bit ADC-DAC.

9.3 ADC-DAC

Among several architectures that exist for implementing ADC circuits, the flash topology is widely employed for achieving high-speed conversion. To achieve n-bit conversion using the flash topology, $2^n - 1$ comparators are required, and therefore improving the resolution of the data converter becomes a challenging task. Different techniques, such as employing time interleaved architectures have been proposed to improve the resolution of the ADC while maintaining a high sampling rate [142], [158]. To date the fastest reported ADC achieves 56 GS/s of sampling rate and 8 bits of resolution [159]. In SiGe technology, the highest sampling rate (40 GHz) belongs to a 3-bit ADC [141]. Other high-speed ADCs in this technology include a 4-bit, 35 GS/s ADC [160], a 5-bit, 22 Gs/s [161] ADC, and a 3-bit, 20 GS/s ADC [162] which incorporates a time-interleaved approach.

Here, we present the design and room temperature measurement results for a 3-bit, 20 GS/s flash ADC, implemented in the 0.12 μm SiGe technology, for the platform intended for conducting extreme environment experiments. For testing purposes, a 7-level thermometer code DAC has been implemented and connected to the digital outputs of the ADC, on the chip.

9.3.1 Design

The block diagram of the 3-bit ADC-DAC is shown in Figure 83. The 3-bit flash ADC consists of a resistor ladder subdividing the $Vref$ voltage into $2^3 - 1$ equal segments, and $2^3 - 1$ comparators. The structure of the comparators is discussed in the previous section and is shown in Figure 78. Each comparator compares the input signal with the fraction of $Vref$ at its input and generates the corresponding logic level. As a result, the ADC converts the input analog signal into 7-level thermometer digital code.

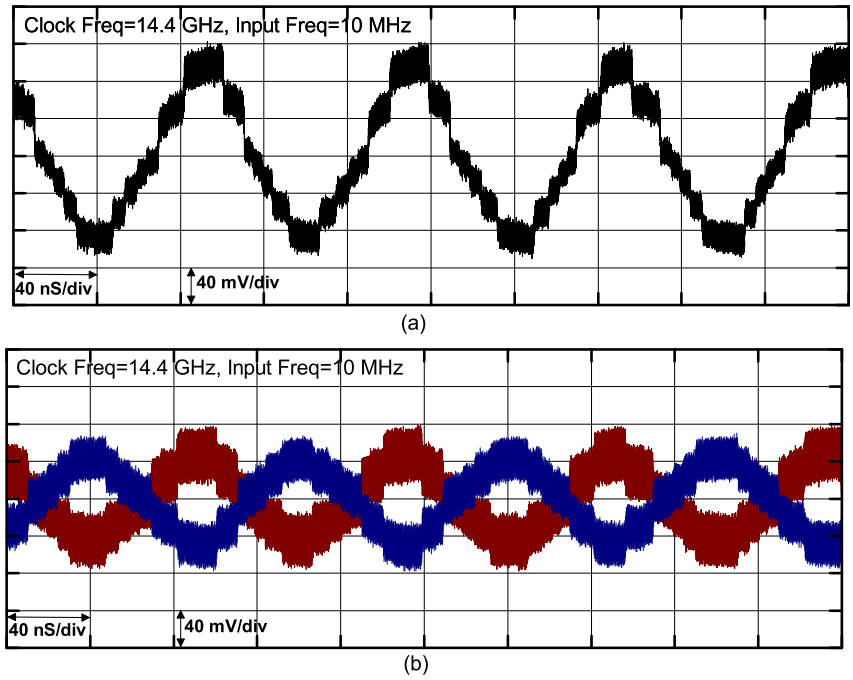

Figure 84: Measured output waveforms of the 3-bit ADC-DAC with a 10 MHz input signal clocking at 14.4 GHz, a)differential output, and b)single-ended outputs. 8 steps of quantization is observed.

A 7-level thermometer code DAC has been implemented on chip, both as a stand-alone circuit, and also directly connected to the output of the ADC to facilitate the testing process. The DAC follows the current-steering topology [155], [163], and consists of 7 HBT-differential pairs designed in current-mode logic configuration and driven by the thermometer codes that are generated at the output of the ADC. The output currents of these CML inverters are summed at the on-chip 50 resistors to reconstruct the input signal sent to the ADC.

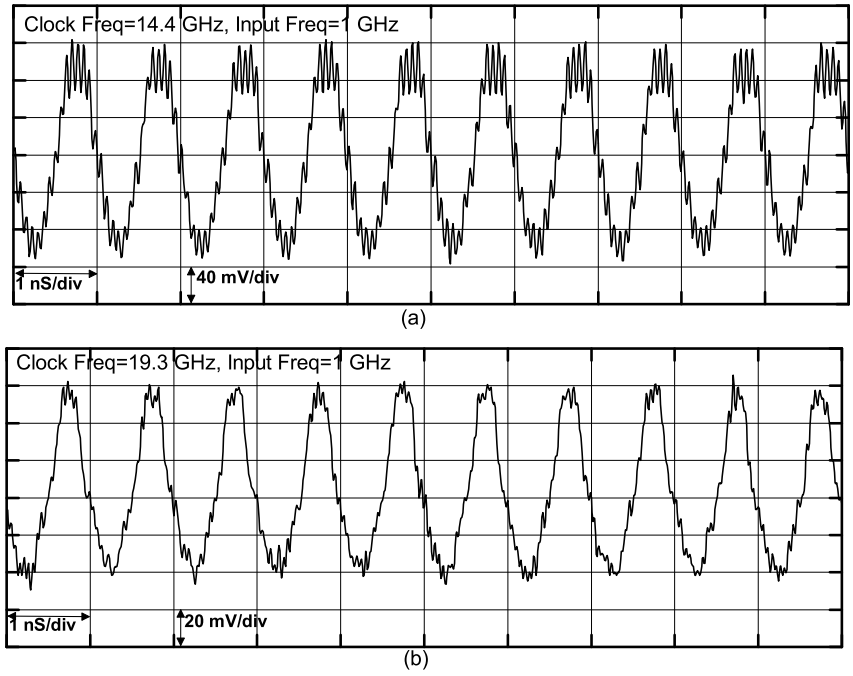

Figure 85: Measured output waveform of the 3-bit ADC-DAC with a 1 GHz input signal clocking at a) 14.4 GHz, and b) 19.3 GHz.

Table 8: Performance Summary and Comparison Table for ADC-DAC

Reference	#Bits/ #Sampling Rate (GHz)	Supply Voltage (V)	Power Dissipation (W)	Architecture	Technology f_T (GHz)	Chip Area (mm^2)
This Work	3/20	2.5	0.1	Flash	SiGe (210)	2.26
[141]	3/40	N/A	4.5	Flash	SiGe (200)	3.96
[160]	4/35	3.3/5	5.1	Flash	SiGe (210)	8.00
[162]	3/20	4.2	2.4	Time Interleave	SiGE (210)	2.55

9.3.2 Measurement Results

40 GHz probes and cables were used for on-wafer measurement. The clock signal to the ADC was generated using an Agilent 83640L continuous wave signal generator. Hybrid and phase tuners were used to convert the single-ended signal into a differential one. A sinusoidal signal with the DC level of 2 V was used as one input to the comparator. The output waveform was captured using 12.5 GHz Tektronix 71254 digital phosphorous oscilloscope. Both ADC and DAC were biased with a 2.5 V supply voltage and the tail currents of the CML inverters inside the DAC were set to 2.5 mA.

Figure 84 shows the measured differential and single-ended outputs of the ADC-DAC for a 10 MHz sinusoidal input signal clocking at 14.4 GHz. The captured time-domain waveforms clearly show 8 quantization levels that verifies proper operation of the 3-bit ADC-DAC circuit. The frequency of the clock signal was increased to 20 GHz and after tuning the setup, the reconstructed sinusoidal signal from the DAC was observable on the Oscilloscope. Figure 85 shows the measured differential output for a 1 GHz signal clocking at 14.4 GHz and 19.3 GHz. The 1-GHz signal is clearly reconstructed, however, the levels of quantization has been reduced. With a power supply of 2.5 V, the 3-bit ADC-DAC circuit consumes 100 mW. Table 8 provides a performance comparison with existing ADC-DAC circuits.

9.4 Extreme Environment Operation

In this section we discuss how low temperature operation and radiation exposure will impact the key performance metrics of the high-speed comparator and the high-speed flash ADC. For the low temperature discussion, it is assumed that the transistors are biased with temperature-independent current and voltage references.

9.4.1 Low Temperature Operation

We will begin with the comparator circuit. As a result of beneficial effects of Ge-grading-induced drift field and lower metal interconnect resistance at reduced temperatures [37], it is expected that the sampling rate of the comparator will improve as the temperature is reduced. With the comparator configuration shown in Figure 78, the input common mode level varies between V_{CC} and $3V_{BE}$. As a result, the input dynamic range of the circuit will be decreased at cryogenic temperatures, since the base-emitter turn-on voltage increases with decreasing temperature. To improve the dynamic range at lower temperatures, one solution is to remove the emitter followers at the input of the preamplifier (Figure 79), at the expense of having larger analog input feedthrough. The resolution of the comparator is limited by the input-referred offset and noise.The main source for the offset voltage is the mismatch between the input transistors, which for two identical transistors can be defined as [155]

$$\Delta V_{BE} = \frac{kT}{q} \ln(1 + \frac{\Delta I_S}{I_S}) \approx \frac{kT}{q} \frac{\Delta A}{A}. \tag{28}$$

In 28, I_S and A are the saturation current and the emitter area, respectively. It can be seen that the offset is a decreasing function of temperature, a good news for low temperature operation. Thermal and shot noise of transistors Q_7-Q_{10} (Figure 79) and the thermal noise of resistors R_3 are the major contributors to the input-referred noise of the comparator. The spectral density of this noise, assuming all the noise

components are uncorrelated, can be expressed as [155]

$$\frac{\nu_n^2}{\Delta f} = 8kT(r_{b7,8} + r_{e7,8} + r_{b9,10} + r_{e9,10} + \frac{1}{2gm_{9,10}} + \frac{1}{gm_{9,10}^2 R_3}, \tag{29}$$

where $r_{b7,8}$, $r_{e7,8}$, $r_{b9,10}$, and $r_{e9,10}$ are the base and the emitter resistances of transistors Q_7/Q_8, and Q_9/Q_{10}, respectively. Equation (29) shows that lowering the temperature will decrease the input-referred noise. In addition, increase in gain of the preamplifier will result in a decrease in both input-referred offset and noise. As shown in equation (26), the gain is improved as the temperature is reduced. Therefore, it is expected that low-temperature operation reduces the the comparators minimum resolvable input voltage and hence, improves its resolution.

The improvements in the performance of comparators at cryogenic temperatures will consequently result in the improvement of the flash ADC's performance. Therefore, it is expected that both the maximum sampling rate and the resolution of the ADC are increased if the circuit operates at lower temperatures. The input signal bandwidth is primarilary limited by the total input capacitance of the ADC. With the preamplifier circuit shown in Figure 79 as the primary stage of each comparator, the base-collector junction capacitance of the input device (Q_7), from each comparator, contributes to the total input capacitance. Cooling effectively reduces this capacitance due to increase in the built-in potential and space-charge region width [164], and therefore, it is expected that the input signal bandwidth of the ADC will be enhanced at low temperature operation.

9.4.2 Radiation Effects

9.4.2.1 Total Ionization Dose Damage

As it was discussed in the previous chapters, TID is SiGe HBTs results in an increase of the non-ideal recombination base current. The choice of the BGR circuit topology becomes important for the reference voltage, as some architectures will be sensitive to the change in the base current of transistors. In addition, increase in the base

current can also negatively impact the integral non-linearity (INL) of the ADC. INL is a metrics for non-linearity error and reduces the effective resolution of the ADC. INL is defined as the maximum deviation of the input/output characteristic from a straight line passed through its end points [155]. As shown in Figure 83, the input of each comparator draws a finite current from the reference ladder, thereby lowering the corresponding tab voltage. Looking at Figure 79, one can realize this finite current is the base current of transistor Q_8. Using Norton equivalents for the resistor ladders, the maximum INL can be shown to be proportional to the base current [155]. Consequently, an increase in the base current after irradiation will result in an increase in the INL, hence decreasing the effective resolution of the ADC. This problem however, can be corrected by injecting corrective currents at one or more points along the ladder.

9.4.2.2 Single Event Transient Effects

It was shown in Chapter 7 that SET in voltage references results in transients in the output voltage. The worst-case SET from the microbeam experiment (with a magnitude of 83.2 mV, FWHM of 64.72 ns) was incorporated into the voltage reference used to set reference values for the 3-bit SiGe ADC. A 500 MHz sinusoidal signal was set to the input and a 12.5 GHz signal was applied to the clock. Shown in Figure 86 are the output waveforms from the ADC-DAC prior to ion strike and during the occurrence of SET in the SiGe voltage source. Figure 86 shows that one quantization step has been missed due to the transient in the voltage reference response. This observation is better explained in Figure 87 for a 2-bit ADC. The input signal is compared to three reference levels at the positive edge of the clock and the corresponding thermometer codes are generated. The SET occurrence in the BGR will result in a time-dependent reference voltage at the input of each comparator. The duration of SET is assumed to be long enough to last 6 clock cycles. The transient

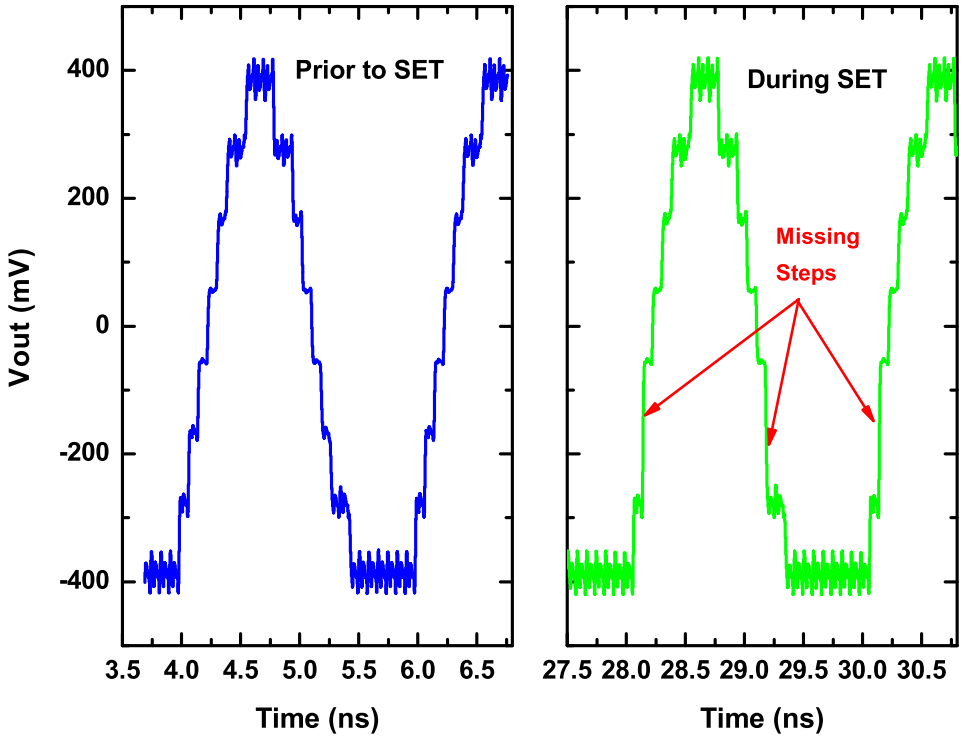

Figure 86: Simulated output waveform of the 3-bit SiGe ADC-DAC; (a) prior to strike (b) during SET.

in the voltage reference shifts the reference points to new levels (red dashed-lines in Figure 87-b), and as a result, the digital output code are corrupted in the first, third, fourth, and the sixth clock cycles. This issue becomes of a greater concern for high resolution ADCs, since the output code will become extremely sensitive to changes in the reference levels.

9.5 Summary

A platform for evaluating the performance of SiGe data converter under extreme environment conditions has been designed and implemented in 0.12 μm SiGe technology. The platform consists of a 25 GS/s comparator, a 3-bit current-steering DAC, and a 3-bit 20 GS/s ADC-DAC. The circuits were measured at room temperature and their

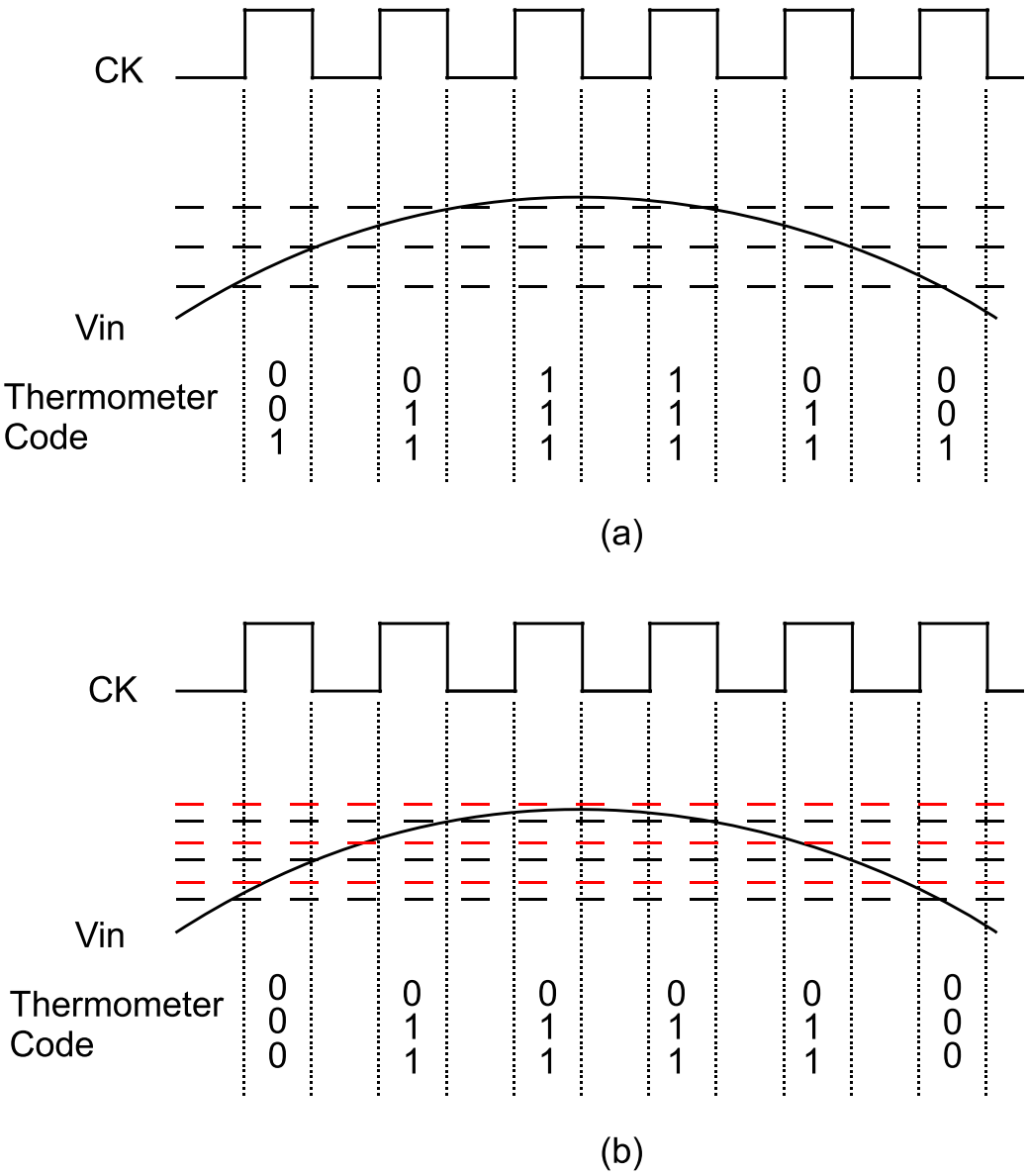

Figure 87: Generation of thermometer codes at the output of a 2-bit ADC; a)before ion strike b) during SET in V_{ref}.

functionalities were verified. Both the stand-alone comparator and the ADC-DAC circuit offer competitive performance with other comparable circuits in the literature while consuming low power consumption. Predictions of the impact of temperature and radiation on the key properties of the comparator and the ADC were provided.

CHAPTER X

CONCLUSIONS AND FUTURE WORK

The theme of this thesis is to explore the potentials of different SiGe technology platforms for implementing analog and mixed-signal circuits with extreme environment capabilities. In this chapter, we summarize the contributions of this dissertation, and provide suggestions for future research directions.

10.1 Contributions

The contributions of this work can be summarized as follows:

1. Several topologies of SiGe BGR circuits with wide-temperature operation capability were successfully realized. The functionality of these circuits were demonstrated over a wide-temperature range of -230° C to 27° C. The impact of the Ge profile shape on BGRs' wide-temperature performance was also studied.

2. The functionality of SiGe HBTs operating in environments below 1 K was demonstrated. A SiGe BGR circuit was also verified to operate reliably at sub-1-K temperatures.

3. The impact of proton irradiation on the performance of SiGe BiCMOS BGR circuits intended for extreme temperature range electronics was investigated. Measurement results were analyzed, and it was shown that the PTAT current generator is the most vulnerable component of the BGR circuit with respect to proton-induced damage.

4. A comprehensive investigation of the performance dependencies of irradiated SiGe voltage reference circuits on TID level, circuit topology, and radiation

source was conducted. The degradation in circuit performance after x-ray irradiation was demonstrated to be dependent on both the circuit topology, and the TID level. It was shown that x-ray exposure of the BGR to large TID levels significantly decreases the magnitude of its output voltage. Detailed analysis was provided to explain the observed anomalies, and the excess base leakage current was identified as the primary factor responsible for the post-irradiation performance degradations. It was also demonstrated that, at the same TID level, x-ray irradiation degrades the circuit performance more than proton irradiation. This radiation-source dependence was also attributed to differences in the excess base current leakage.

5. Single-event transient responses of SiGe BGR circuits were examined through heavy ion microbeam experiment. It was shown that depending on the location of the strike, the magnitude and the duration of the transients vary from one event to another. Sensitive transistors responsible for creating large and long transients were identified in the BGR circuit.

6. The impact of proton irradiation on the DC performance of HV transistors, implemented in a LV SiGe technology, was throughly investigated. The effects of irradiation gate bias, irradiation substrate bias, and the operating substrate bias, on the radiation response of these HV transistors were studied. It was observed that the level of radiation-induced leakage current in HV transistors is significantly smaller than the level of radiation-induced leakage current in their LV counterparts, suggesting that the mechanisms involved in causing radiation-induced degradation, in LV and HV transistors, could be of fundamentally different origins.

7. A test platform consisting of a low-power high-speed comparator, a 3-bit DAC, and a low-power high-speed 3-bit flash ADC-DAC, was realized in third-generation

SiGe BiCMOS technology. The circuits were successfully characterized at room temperature and the impact of extreme environment operation on their key electrical properties was discussed.

10.2 Future Work

This work establishes several interesting research directions for future work:

1. Investigating the impact of Ge profile and B base profile shapes on the wide-temperature performance of mixed-signal circuits through simulation and conducting experiments.

2. Developing new architectures for BGR circuits that are tolerant to x-ray exposure.

3. Designing experiments for understanding the physics beyond the operation of SiGe HBTs at mK temperatures.

4. Utilizing mixed-mode simulation for the prediction of the SET response of analog and mixed-mode circuits.

5. Understanding the mechanisms involved in causing radiation-induced degradation in HV transistors.

6. Investigating low-temperature operation and the radiation response of high-speed data converters.

7. Realizing low-power high-speed data converters with improved resolution.

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