Zeroing in On a Zero-Temperature Coefficient Point

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***Abstract*—The transconductance characteristics of MOS transistors realized in 0.18 μm CMOS technology have a zero-temperature coefficient (ZTC) bias point. The presence of this point influences performance of both analog and digital circuits. The offset voltage drift in a source-coupled differential pair strongly increases, if the transistor drain currents are equal to the bias currents of ZTC point. It is also impossible to find the drain voltage optimizing the temperature stability of propagation delay in digital circuits. One has to divide the digital circuits in two types. In the first type (CPU circuits) the optimal drain voltage is equal to ZTC bias point voltage of n-channel transistors, in the second case (SRAM circuits) the optimal drain voltage is equal to the absolute value of the ZTC bias point voltage of p-channel transistors.**

***Key words*: MOSFET, device characterization, temperature effects, offset voltage drift, propagation delay temperature stability**

I. Introduction

Fig. 1 shows the simulated transconductance characteristics, with the temperature as a parameter, of two transistors designed in 0.18 μm CMOS technology. One can see that the characteristics have a common intercept point (for p-channel transistor this point is not so well defined). If transistor is biased to this point by a current source, then the gate-source voltage will not depend on temperature. This is the zero-temperature coefficient (ZTC) point [1]. It occurs when the transistor has mutual compensation of mobility and threshold voltage temperature effects. This compensation exists for a series of industrial n^+-polysilicon gate CMOS process technologies [2, 3].

The ZTC point can be used for design of temperature stabilized voltage [3] and current [4] sources. From the other side, operation of transistors with voltages and currents below ZTC point may cause the thermal run-out and destruction of digital circuit [5]. Hence, the ZTC point influences performance of both analog and digital circuits.

In this paper we discuss two questions. For analog circuits we show that the offset voltage drift in a source-coupled differential pair strongly increases, if the transistor drain currents happen to be equal to the bias currents of ZTC point. In this case the drift components of individual transistors are added.

For digital circuits we show that it is impossible to find the drain voltage optimizing the temperature stability of propagation delay. One has to divide the digital circuits in two types. In the first case (CPU circuits) the optimal drain voltage is equal to the ZTC bias point voltage of n-channel transistors, in the second case (SRAM circuits) the optimal drain voltage is equal to the absolute value of the ZTC bias point voltage of p-channel transistors.

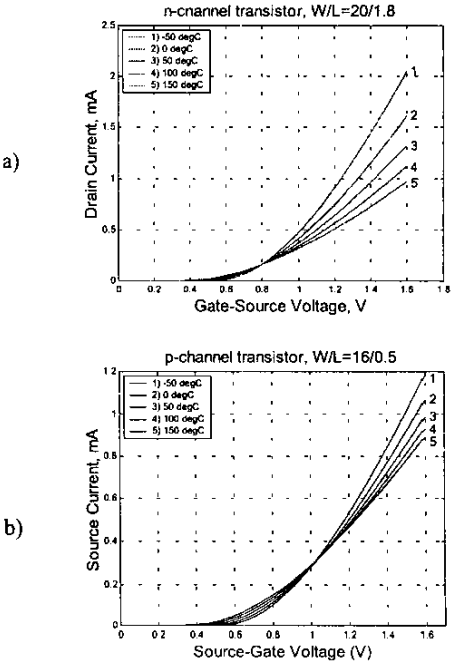

Fig. 1 Simulated transconductance characteristics
a) n-channel transistor, b) p-channel transistor

Part II of this work reviews the mutual compensation of mobility and threshold voltage temperature effects in MOS FETs, when it results in a ZTC bias point. Part III considers calculation of the differential pair offset voltage drift. Part IV considers the temperature dependence of the propagation delay, and the conditions of optimal choice of the circuit power supply voltage. Part V describes our experimental results pertaining to the analog circuits (the experimental confirmation of the results pertaining to digital circuits can be found in earlier work, in [6] for simulations and in [7] for experiments).

II. Compensation of Mobility and Threshold Voltage Temperature Effects

The transconductance characteristics of a (n-channel) MOS transistor are described by the equation

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$$I_D = (1/2)\mu_n C_{ox}(W/L)(V_{GS} - V_{Tn})^2 . \quad (1)$$

The carrier mobility, μ_n, and the threshold voltage, V_{Tn}, are temperature dependent parameters. Both of them decrease with temperature. The threshold voltage depends on temperature [8] as

$$V_{Tn}(T) = V_{Tn}(T_0) + \alpha_{Tn}(T - T_0) \quad (2)$$

(α_{Tn} is negative), and the mobility [9] as

$$\mu_n(T) = \mu_n(T_0)(T/T_0)^{-m} \quad (3)$$

(m is positive). Here T_0 is the reference temperature (300°K). If $m = 2$ then one effect compensates another, and the characteristics will have a common intercept point (V_{GSF}, I_{DF}). As shown in [3,4] the parameters of this point are

$$V_{GSF} = V_T(T_0) - \alpha_{Tn} T_0 \quad (4)$$

and

$$I_{DF} = (1/2)\mu_n(T_0) C_{ox} T_0^2 (W/L)\alpha_{Tn}^2 . \quad (5)$$

If equations (4) and (5) are substituted in (2) one obtains that

$$V_{GS} = V_{GSF} + \alpha_{Tn} T\left[1 - \sqrt{\frac{I_D / I_{DF}}{(T/T_0)^{2-m}}}\right]. \quad (6)$$

When $m = 2$ then (6) is simplified to

$$V_{GS} = V_{GSF} + \alpha_{Tn} T(1 - \sqrt{I_D / I_{DF}}) . \quad (7)$$

This result shows that in case of a constant drain current the gate-source voltage is proportional to temperature. This voltage can be increasing with temperature if $I_D > I_{DF}$, or decreasing if $I_D < I_{DF}$. Fig. 2 shows the simulation results (solid lines) and calculations (star lines) obtained for the transistor with aspect ratio of W/L=20μm/1.8μm. The calculations, in accordance with (7) using $V_{GSF} = 800\,\text{mV}$ and $I_{DF} = 162\,\mu\text{A}$ are also shown as star dots). The calculated and simulated results are in a good agreement, and confirm that, indeed, m should be reasonably close to 2.

Similar results can be obtained for p-channel transistors.

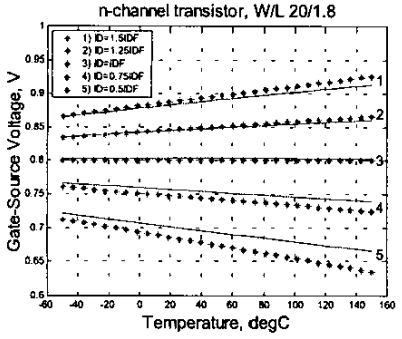

Fig. 2 Gate-source voltage temperature dependence with the drain current as a parameter

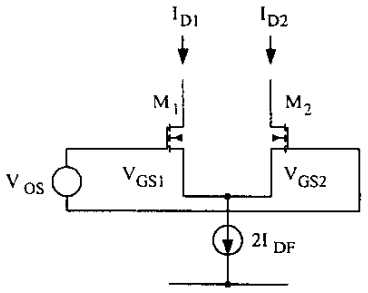

Fig. 3 Source-coupled transistor pair

III. Offset Voltage Drift

The result (7) can be used now for calculation of the differential pair offset voltage and offset voltage drift. Assume that we have a pair of identical transistors (Fig. 3) biased by the tail current $2I_{DF}$. Yet, let their drain currents, for some reasons be different. Then the offset voltage, V_{OS}, will be

$$V_{OS} = V_{GS1} - V_{GS2} = \alpha_{Tn} T\left(\frac{\sqrt{I_{D2}} - \sqrt{I_{D1}}}{\sqrt{I_{DF}}}\right) \quad (8)$$

The offset voltage drift can be found now as

$$\frac{\partial V_{OS}}{\partial T} = \alpha_{Tn}\left(\frac{\sqrt{I_{D2}} - \sqrt{I_{D1}}}{\sqrt{I_{DF}}}\right) \quad (9)$$

This result shows, contrary to [10], that there is no first order cancellation of V_{GS} temperature variations. In fact, when $I_{D1} < I_{DF}$ and $I_{D2} > I_{DF}$, the temperature variations are added, as it follows from the derivation.

As an example consider the differential pair that includes two n-channel transistors with W/L=20μm/3.3μm realized in 0.18 μm CMOS technology with the process parameters $\mu_n C_{ox}$=190μA/V^2 and $V_{Tn}(T_0)$=400mV. We obtained, in simulations, that these transistors have V_{GSF} = 787mVand I_{DF}=90μA. If this pair is biased by the tail current of $2I = 2I_{DF}$=180μA, and the drain currents are I_{D1}=63μA and I_{D2}=117μA, then, using (4) one finds that $\partial V_{OS}/\partial T$ = - 0.39mV/° (-0.32mV/°C in simulations for the temperature range of -40 to 150 °C).

IV. Temperature Variation of Propagation Delay

Let us consider a simple CMOS inverter (Fig. 4, a). Assume that the rise-time delay is defined from Fig 4, b, when the p-channel transistor operates in saturation. Similarly, let the fall-time delay be defined from Fig. 4, c, when the n-channel transistor operates in saturation. Then the propagation delay is defined [11] as

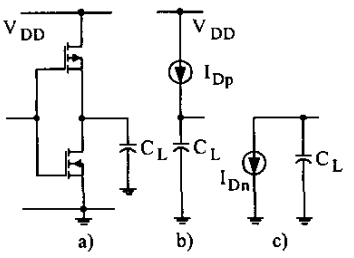

Fig. 4 CMOS inverter (a) and equivalent circuits for calculation if the rise-time (b) and fall-time (c)

$$\tau_d = \frac{C_L V_{DD}}{2C_{ox}}\left(\frac{1}{F_p}+\frac{1}{F_n}\right)=\frac{C_L V_{DD}(F_p+F_n)}{2C_{ox}F_pF_n}. \quad (10)$$

Here $F_p = \mu_p (W/L)_p (V_{DD}-|V_{Tp}|)^2$ and $F_n = \mu_n (W/L)_n (V_{DD}-V_{Tn})^2$. For small variations of temperature one can assume that

$$\tau_d \approx \tau_d(T_0) + K_{Td}\Delta T \quad (11)$$

where $\Delta T = T - T_0$ and

$$K_{Td}\Delta T \approx \frac{C_L V_{DD}(\Delta F_p + \Delta F_n)}{2C_{ox}F_p(T_0)F_n(T_0)}. \quad (12)$$

One may rewrite (2) and (3) as

$$\begin{cases} \mu_n = \mu_n(T_0)\left(1+\dfrac{\Delta T}{T_0}\right)^{-m_n} \\ V_{Tn} = V_{Tn}(T_0)+\alpha_{Tn}\Delta T \end{cases}. \quad (13)$$

Assume that the temperature dependencies of mobility and threshold voltage are similar, i. e.

$$\begin{cases} \mu_p = \mu_p(T_0)\left(1+\dfrac{\Delta T}{T_0}\right)^{-m_p} \\ |V_{Tp}| = |V_{Tp}(T_0)|+\alpha_{Tp}\Delta T \end{cases}. \quad (14)$$

Substituting (13) and (14) in (12) and assuming that the usual [11] design condition

$$\mu_p(T_0)(W/L)_p = \mu_n(T_0)(W/L)_n = K_\mu \quad (15)$$

is satisfied one can find that

$$\Delta F_p + \Delta F_n = -K_\mu (V_{DP}+V_{DN}), \quad (16)$$

where

$$V_{DP} = [V_{DD}-|V_{Tp}(T_0)|]\left[\left(\frac{m_p}{T_0}\right)[V_{DD}-|V_{Tp}(T_0)|]+2\alpha_{Tp}\right] \quad (17)$$

and

$$V_{DN} = [V_{DD}-V_{Tn}(T_0)]\left[\left(\frac{m_n}{T_0}\right)[V_{DD}-V_{Tn}(T_0)]+2\alpha_{Tn}\right]. \quad (18)$$

Hence, the temperature-insensitive inverter operation requires that the following conditions are satisfied

$$\begin{cases} (m_p/T_0)[V_{DD}-|V_{Tp}(T_0)|]+2\alpha_{Tp}=0 \\ (m_n/T_0)[V_{DD}-V_{Tn}(T_0)]+2\alpha_{Tn}=0 \end{cases}. \quad (19)$$

From (19) one can find that the optimal power supply voltage should be chosen from two values

$$\begin{cases} V_{DD} = |V_{Tp}(T_0)| - (2\alpha_{Tp}T_0)/m_p \\ V_{DD} = V_{Tn}(T_0) - (2\alpha_{Tp}T_0)/m_n \end{cases}. \quad (20)$$

If $m_p = m_n = 2$ (i.e. the ZTC points exist for both p-channel and n-channel transistors; this condition is not always satisfied) then (20) is reduced to

$$\begin{cases} V_{DD} = |V_{Tp}(T_0)| - \alpha_{Tp}T_0 = |V_{GSFp}| \\ V_{DD} = |V_{Tn}(T_0)| - \alpha_{Tn}T_0 = V_{GSFn} \end{cases}. \quad (21)$$

In general, the figures of $|V_{FSGp}|$ and V_{GSFn} are different. The simulations show that for 0.18μm CMOS technology $|V_{FSGp}|$ is about 800 mV, and V_{GSFn} is about 1V (see Fig. 1). The dependence of these figures on transistor size and aspect ratio is weak (ideally, in accordance with (4) they should be the process parameters). One has to divide the digital circuits in two types (here we follow [7]. In the first type (CPU circuits) the optimal drain voltage is equal to V_{GSFn}, in the second case (SRAM circuits) the optimal drain voltage is equal to $|V_{FSGp}|$. If the circuit is a mixture of both types of circuits the optimal V_{DD} voltage is in-between of these two figures.

V. Experimental Results

A simple circuit (Fig. 5) was designed, manufactured and tested to verify the developed results. The circuit includes an operational amplifier (transistors M_4 to M_{10}) with 100% negative feedback and a positive feedback via current mirror M_{11}, M_2 and the diode-connected transistor M_1. The amplifier is compensated with a 530 fF capacitor. The load of the operational amplifier consists of two resistors R_p and R_n. An additional diode-connected n-channel transistor M_{13} is also included.

The circuit was designed for 0.18 μm CMOS technology with the following process parameters: the threshold voltages are $V_{TN} = 400$ mV, $V_{TP} = -480$ mV, $\mu_n C_{ox} = 190\,\mu A/V^2$, $\mu_p C_{ox} = 47\,\mu A/V^2$, $\gamma_n = 0.498\ V^{1/2}$, $\gamma_p = 0.575\ V^{1/2}$. The surface potential is $2|\phi_f| = 0.65$ V for both types of transistors. The resistor R_p=2.46 kΩ is realized using n^+-diffusion layer and has positive temperature coefficient of TC_p=1.47*10^{-3}. The resistor R_n=2.48 kΩ is realized using n^+-polysilicon layer and has negative temperature coefficient of TC_n=-1.46*10^{-3}.

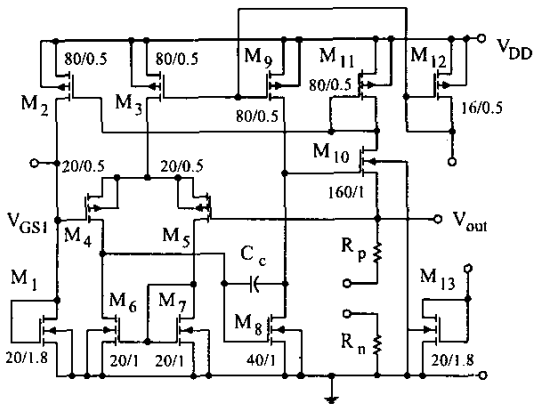

Fig. 5 Experimental circuit

The circuit was used for the following experiments.

1) Applying externally different constant currents to transistors M_{12} or M_{13} we obtained the characteristics shown in Fig. 2, hence we verified the presence of ZTC points in these transistors.

2) Connecting R_p and R_n in series one obtains a resistor with practically zero temperature coefficient. The circuit is designed so that in this case M_1 is biased to its ZTC point and the voltage V_{out} should not depend on temperature. The experiment shows a weak dependence (0.3 mV/°C in the range of 22 to 140°C).

3) Monitoring the differential pair offset we were able to verify the linear dependence of offset voltage with temperature and confirm the offset drift prediction (0.015mV/ °C for the initial offset of 0.9 mV at 22 °C).

The circuit is powered by $V_{DD} = 1.8$ V. The bias current is 10 μA. The results of above given tests are in a reasonable agreement with that of calculations and simulations.

VI. Discussion and Conclusions

Most of the calculated results in this paper are based on the assumption that $m_p = m_n = 2$. These values are more feasible for the level of substrate doping in modern technologies (about 10^{15} to 10^{16} cm^{-3}) than the frequently used value of -1.5. More discussion can be found in [3,4].

If transconductance characteristics have ZTC bias point then the diode-connected transistor has nearly linear temperature dependence of the gate-source voltage when this transistor is biased with a current source or even a resistor. Such transistor can be used as a temperature sensor. The slope of the temperature dependence can be controlled by the bias current.

The ZTC bias point can be also used to create a reference voltage and current that can be used for temperature stable bias.

Finally, the ZTC bias point voltage determines the optimal V_{DD} voltage in the digital circuits for temperature insensitive operation.

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