A SIMPLE VOLTAGE REFERENCE USING TRANSISTOR WITH ZTC POINT AND PTAT CURRENT SOURCE

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ABSTRACT

When a diode-connected MOS transistor is biased with a PTAT current source, the gate-source voltage of such transistor can be temperature independent. Based on this idea a circuit is designed and implemented in a standard 0.18-μm CMOS technology. The simulations show that the output voltage of this reference has the temperature coefficient of 4 ppm/°C in the range of $-50°C$ to $150°C$. If this transistor is biased below the zero temperature coefficient (ZTC) point this technique opens the way to design a sub-1 V voltage reference.

Keywords: Analog electronics, voltage references, mobility, threshold voltage, temperature effects

1. INTRODUCTION

The presence of the zero temperature coefficient (ZTC) point in MOS transistors, where one has mutual compensation of mobility and threshold voltage temperature effects, is known [1]. This effect exists in many technologies [2] and has found some applications in design of voltage references [3]. It was shown in [2] that using a constant current for biasing a diode-connected transistor at the ZTC point, a temperature-stable gate-source voltage can be obtained. The reported temperature coefficient was 13 ppm/°C in the range of 0°C-125°C. Yet, the realization of a temperature independent current source is difficult. Here, we show that using a proportional to absolute temperature (PTAT) bias current, which is much easier to realize than a temperature independent current source, it is possible to obtain a temperature independent gate-source voltage when the transistor is biased below its ZTC point. In addition, this result can be employed to develop a sub 1-V temperature-independent reference voltage.

This paper is organized as follows. In Section 2, we assume that a diode-connected MOS transistor is biased with a PTAT current source. We find the design conditions for the PTAT current source, which make the sgate-source voltage of the diode-connected MOS transistor temperature independent. In Section 3, these conditions are used for the design of a PTAT current source biasing a diod-connected NMOS transistor. Simulation results based on the circuit proposed in Section 3 are given in Section 4. Finally, the results of the paper are summarized in Section 5.

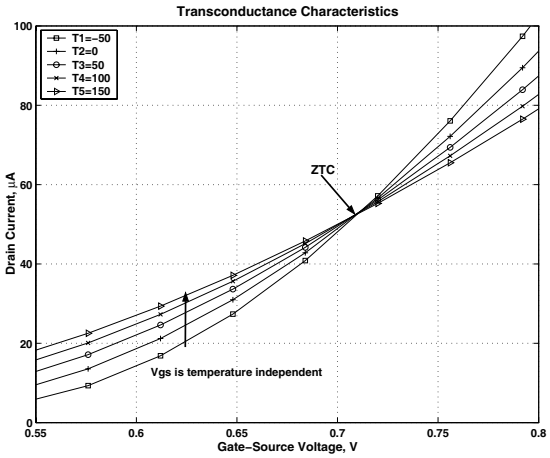

Fig. 1. Simulated transconductance characteristics of a NMOS transistor

2. DIODE-CONNECTED NMOS TRANSISTOR OPERATION WITH PTAT DRAIN CURRENT

Fig. 1 shows the simulated transconductance characteristics (with temperature as a parameter) for a NMOS transistor in 0.18-μm CMOS technology. The ZTC point is clearly shown in the figure. Let this transistor be diode connected and biased with the PTAT current, $I_D(T)$, i.e.,

$$I_D(T) = I_{D0}[1+\gamma(T-T_0)] \tag{1}$$

where γ is a positive constant. For a MOS transistor in saturation, the drain current can be expressed as [4]

$$I_D = \frac{\mu C_{ox}}{2}\left(\frac{W}{L}\right)(V_{GS}-V_{TH})^2. \tag{2}$$

The mobility, μ, and the threshold voltage, V_{TH}, are temperature dependent parameters. The temperature dependency of the mobility, μ, is given as [5]

$$\mu = \mu_0 (T/T_0)^{-m} \tag{3}$$

where T_0 is the reference temperature and m is a positive constant in the range of 1.5 to 2 [3],[5]. The threshold voltage, V_{TH}, linearly decreases with temperature as [6]

$$V_{TH} = V_{TH0} - \alpha_{VT}(T - T_0) \tag{4}$$

where α_{VT} is a positive constant and is in the range of (1.5 to 2) mV/°C [6]. Substituting (3) and (4) in (2) and solving for V_{GS} we obtain

$$V_{GS}(T) = V_{TH0} - \alpha_{VT}(T - T_0) + K(\frac{T}{T_0})^{\frac{m}{2}} \sqrt{I_D(T)} \tag{5}$$

where

$$K = \sqrt{\frac{2}{\mu_0 C_{ox}(W/L)}}. \tag{6}$$

Let the temperature increase from $T = T_0$ by a small amount of δT to $T_0 + \delta T$. Substituting (1) in (5) and using the approximations

$$\sqrt{(1+\gamma\delta_T)} \cong 1 + (\gamma\delta T)/2 \tag{7}$$

and

$$(1 + \frac{\delta T}{T_0})^{\frac{m}{2}} \cong 1 + \frac{m}{2}\frac{\delta T}{T_0} \tag{8}$$

one obtains that the change in the gate-source voltage, δV_{GS} , is equal to

$$\delta V_{GS} = V_{GS}(T_0 + \delta T) - V_{GS}(T_0) \cong \delta T[-\alpha_{VT} + \frac{\lambda}{2}(\frac{m}{T_0} + \gamma)] \tag{9}$$

where $\lambda = K\sqrt{I_{D0}}$. Hence, if a PTAT current source has the design parameters λ and γ satisfying

$$\frac{\lambda}{2}(\frac{m}{T_0} + \gamma) = \alpha_{VT} \tag{10}$$

then the gate-source voltage of the diode-connected transistor biased with this current source, can be temperature independent.

3. CIRCUIT STRUCTURE

Fig. 2 shows a diode-connected transistor, M_6, biased with a PTAT current source (transistors $M_1 - M_5$ and resistor R_B). The standard low-voltage bias circuit, given in [4], is used to generate the PTAT current for the diode-connected transistor. Transistors M_{s1}-M_{s3} form the start-up circuit.

We now show that the standard bias circuit, consisting of transistors M_1-M_4 and resistor R_B, generates a PTAT current. Assuming $R_B = R_{B0}[1 + \alpha_{R1}(T - T_0) + \alpha_{R2}(T - T_0)^2]$

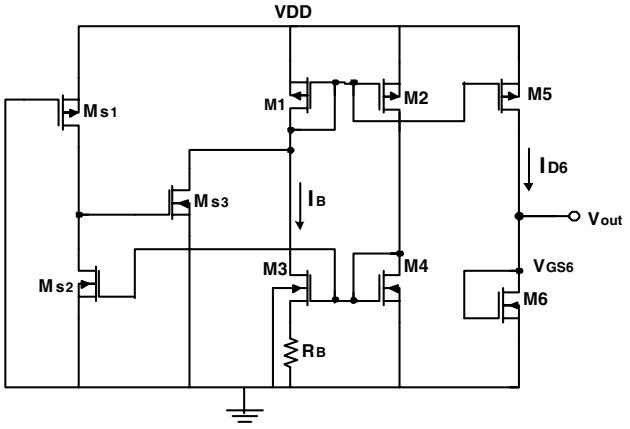

Fig. 2. Diode-connected transistor biased with PTAT current source

and using a first order approximation, one can find that the loop current, I_B, in the bias current is equal to

$$I_B \cong I_{B0}[1 + \gamma(T - T_0)] \tag{11}$$

where

$$I_{B0} = (2/C_{ox})\mu_0^{-1} R_{B0}^{-2} \left(\sqrt{(L/W)_4} - \sqrt{(L/W)_3}\right)^2 \tag{12}$$

and

$$\gamma = \frac{m}{T_0} - 2\alpha_{R1} \tag{13}$$

are temperature independent parameters.By using N^+ non-silicide diffusion layer with $\alpha_{R1} = 1.47 \times 10^{-3}\text{deg}^{-1}$ for the realization of the resistor, one obtains γ a positive value in the range of ($2 \times 10^{-3}\text{deg}^{-1}$ to $3.7 \times 10^{-3}\text{deg}^{-1}$). The current that biases Transistor M_6 becomes equal to

$$I_{D6} = I_{D60}[1 + \gamma(T - T_0)] \tag{14}$$

where $I_{D60} = \left((\frac{W}{L})_5/(\frac{W}{L})_1\right) I_{B0}$.

In order to have a temperature-independent gate-source voltage, equation (10) should be satisfied. Substituting (13) in (10) one obtains

$$\lambda(\frac{m}{T_0} - \alpha_{R1}) = \alpha_{VT} \tag{15}$$

where $\lambda = K_6\sqrt{I_{D60}}$. Therefore if the sizes of transistors M_1 and M_5 satisfy

$$\sqrt{\frac{(W/L)_5}{(W/L)_1}} = \frac{\alpha_{VT}}{K_6\sqrt{I_{B0}}(\frac{m}{T_0} - \alpha_{R1})}, \tag{16}$$

then the gate-source voltage, V_{GS6}, will be temperature independent.

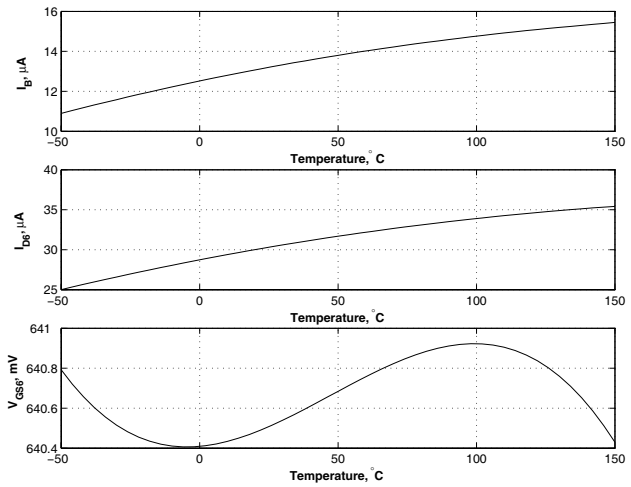

Fig. 3. Diode-connected transistor biased with PTAT current source

4. SIMULATION RESULTS

The circuit shown in Fig. 2 was designed for realization in 0.18-μm TSMC technology. The value of the resistor and the sizes of the transistors are given in Table 1.

The circuit was simulated in the temperature range of -50°C to 150°C using a power supply voltage of 1.8 V. However, since the minimum required power supply is equal to

$$V_{DD_{\min}} = (V_{THn})_{\max} + |V_{DS5}(\text{sat})| \tag{17}$$

the circuit is able to operate with a sub-1 V power supply.

Fig. 3 shows the simulation results for the PTAT currents, I_B and I_6 and the gate-source voltage V_{GS6}. The temperature stability of the gate-source voltage, V_{GS6}, obtained in simulations is equal to 4 ppm/$^{\circ}$C. A more exact analysis shows that (11) includes also the second order nonlinearity term with the dominating component of $-(2m\alpha_{R1}/T_0)(T-T_0)^2$ that results in not an exact realization of PTAT current and the residual temperature dependence of the gate-source voltage as shown in Fig. 3. The results of simulation verify that the circuit operates according to the analysis given in Sections 2 and 3. The circuit has been sent for fabrication and will be ready in 4 months for experimental measurements.

5. DISCUSSIONS AND CONCLUSIONS

It was shown that using a PTAT current source, it is possible to obtain a temperature independent gate-source voltage from a diode-connected transistor biased below its ZTC point. A circuit based on this idea was designed and simulated. The temperature coefficient of the output voltage of the proposed circuit is 4 ppm/$^{\circ}$C in the range of -50°C-150°C. The minimal required power supply voltage is equal to $V_{THn} + |V_{DS5,\text{sat}}|$, and the circuit can be easily designed with the saturation voltage, $V_{DS,\text{sat}}$ less than 0.2 V. Therefore, the technique presented here can be used to develop sub-1 V CMOS voltage references. At the present time, we do not have experimental data (we hope to have them to the time of symposium). But even if they will be 10 times worse than the results in simulations, the proposed circuit will be still comparable with other circuits designed for lower than 1 V power supply [7].

Table 1. Transistor and Resistor sizes

M_{s1}	M_{s2}	M_{s3}	M_1	M_2
$\frac{.42\mu}{2\mu}$	$\frac{10\mu}{2\mu}$	$\frac{3\mu}{2\mu}$	$\frac{8\mu}{2\mu}$	$\frac{8\mu}{2\mu}$
M_3	M_4	M_5	M_6	R_B
$\frac{5.5\mu}{2\mu}$	$\frac{4\mu}{2\mu}$	$\frac{18.4\mu}{2\mu}$	$\frac{8\mu}{2\mu}$	$2k\Omega$

6. REFERENCES

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