SiGe BiCMOS Precision Voltage References for Extreme Temperature Range Electronics

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***Abstract* — We present the first investigation of the optimal implementation of SiGe BiCMOS precision voltage references for extreme temperature range applications (+120 °C to -180 °C and below). We have developed and fabricated two unique Ge profiles optimized specifically for cryogenic operation, and for the first time compare the impact of Ge profile shape on precision voltage reference performance down to -180 °C. Our best case reference achieves a 28.1 ppm/ °C temperature coefficient over +27 °C to -180 °C, more than adequate for the intended lunar electronics applications.**

***Index Terms* — analog circuits, SiGe HBT, cryogenic temperature, voltage reference, device physics.**

I. Introduction

For many space exploration applications, it is highly desirable to have electronic components capable of operating robustly over extreme temperature ranges, since it can profoundly improve robotic system architecture and performance, reduce system power drain, dramatically reduce launch weight, and improve overall mission reliability. On the surface of the Moon (NASA's next mandated exploration venue), for example, ambient temperatures range from +120 °C (lunar day) to -180 °C (lunar night), and even down to -230 °C (shadowed polar craters). Designing robust electronic systems for > 300 °C (cyclic) temperature variations has never been attempted, until now. Bandgap-engineered SiGe heterojunction bipolar transistors (SiGe HBTs) are known to have superior performance down to deep cryogenic temperatures [1] and therefore have recently emerged as a leading contender for such extreme temperature range electronics applications. SiGe IC design platforms offer both high speed SiGe HBTs and Si CMOS, and a host of passive elements for developing highly-integrated system-on-a-chip and system-in-a-package components for use in emerging lunar electronic systems. SiGe HBTs have a desirable side benefit of possessing a natural hardness to ionizing radiation (a key concern for most space applications).

Key to the success of this vision of developing extreme temperature range electronics is to realize a robust precision voltage reference. Voltage references (e.g., bandgap voltage references - BGR) are used extensively in space electronic systems for A/D and D/A converters, voltage regulators, and many other mixed-signal circuits, and can be viewed as a necessary (and inherently difficult) analog primitive for the successful realization of this vision. Simply stated, if robust voltage references cannot be achieved, all bets are off for developing extreme temperature range systems.

We present here the first investigation of the optimal implementation of SiGe BiCMOS precision voltage references for such extreme temperature range applications, and demonstrate that SiGe BiCMOS can indeed achieve the necessary performance for

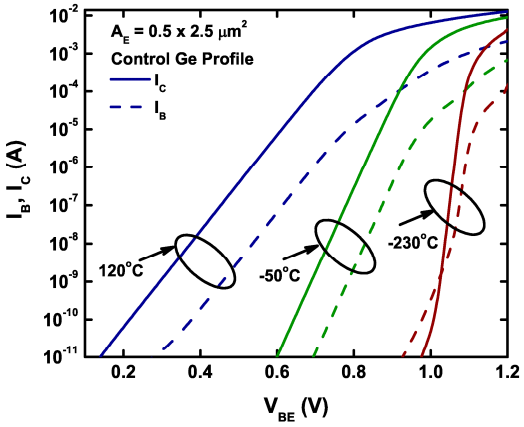

Fig.1. Gummel characteristics at +120°C, -50°C, and -230°C for a 0.5×2.5 μm² SiGe HBT.

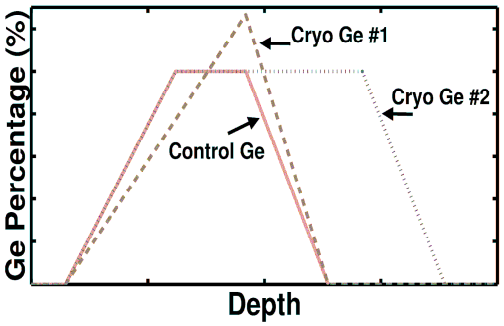

Fig. 2. Shapes of the three Ge profiles used.

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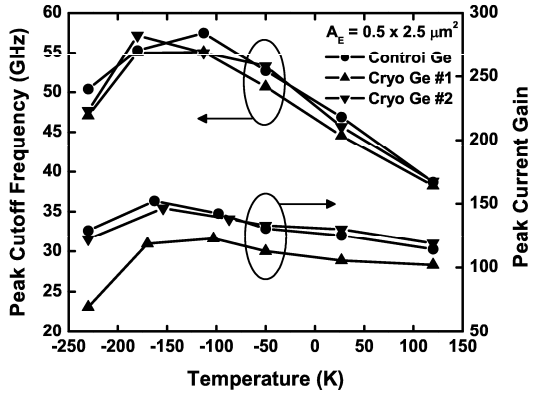

Fig. 3. Measurement results for the maximum current gain and peak f_T as a function of temperature for three Ge profiles.

lunar electronics systems. In addition, we have developed and fabricated two unique Ge profiles optimized specifically for cryogenic operation, and for the first time compare the impact of Ge profile shape on precision voltage reference performance over temperature.

II. SiGe HBT BiCMOS Technology

The SiGe technology platform used here is the commercially-available IBM 5AM SiGe BiCMOS technology, featuring 0.5 μm, 50 GHz (27 °C) SiGe HBTs. Fig. 1 shows the Gummel characteristics of a 0.5×2.5 μm^2 SiGe HBT at 120 °C, -50 °C, and -230 °C (the lowest temperature for lunar applications). Due to the exponential decrease of the intrinsic carrier concentration with cooling, the base-emitter turn-on voltage increases as the temperature decreases, as expected. At -230 °C, this device has a maximum current derive in excess of 4mA/μm^2. We call the Ge profile used in this commercial technology the "Control Ge" profile. A comparison of the three Ge profiles used in this investigation is shown in Fig. 2. "Cryo Ge #1" and "Cryo Ge #2" are the optimal cryogenic profiles that were designed based upon calibrated 2-D simulations over temperature, with constant stability and deeper retrograding, respectively (the latter to improve immunity to heterojunction barrier effect). The shape of the Ge profile at the base-emitter side for both the conventional Cryo Ge #2 and the Control Ge profile is similar. Measurement results for the peak current gain and peak cutoff frequency as a function of temperature for the three Ge profiles are shown in Fig. 3. As can be seen, all three Ge profiles exhibit excellent characteristics down to -230 °C, while the two optimized Ge profiles give significantly better *DC* and *AC* performance at peak f_T and into high injection, as intended.

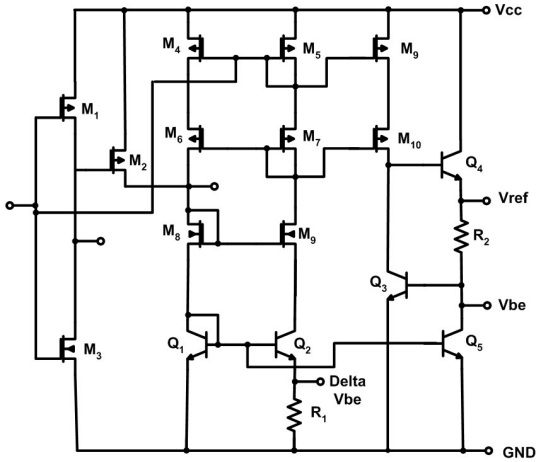

Fig. 4. Schematic of the SiGe voltage reference.

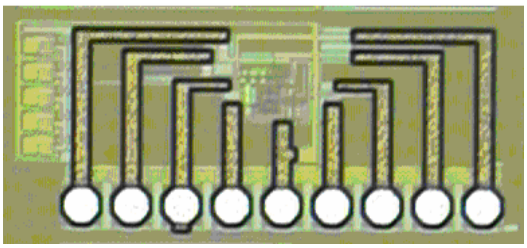

Fig. 5. Die micrograph of the SiGe voltage reference.

III. Circuit Design

The BGR implemented for this investigation is based on an exponential curvature compensation technique [2] and exploits the temperature characteristics of the current gain of the SiGe HBT for curvature compensation. To enable meaningful circuit design, the calibrated VBIC models within the design kit were first modified and fit to low temperature transistor data. The schematic of the BGR circuit is shown in Fig. 4. Each of the bipolar transistors shown in this figure, except for Q_2, consists of four parallel copies of the 0.5×2.5 μm^2 SiGe HBT. The area of transistor Q_2 is eight times larger than that of the other transistors. Transistors M_1-M_3 comprise the startup circuit, and transistors M_4-M_9 and Q_1-Q_2, along with the resistor R_1, generate the proportional to the absolute temperature (PTAT) bias current for the other stages. Several pads have been inserted to monitor the nodes of some of the transistors inside the circuit as the temperature was varied. The circuit was designed for a power supply voltage of 3.3 V. With the pads, the circuit occupies an area of 1.3×0.4 mm^2 (Fig. 5). Careful layout techniques were employed to reduce mismatch effects.

IV. Experimental Results & Discussion

The circuits were mounted in a 28 pin ceramic package, wire-bonded, and placed inside a closed-cycle helium cryostat for characterization.

TABLE I
SUMMARY

	Control Ge		Cryo Ge #1		Cryo Ge #2	
Vref (V)	1.1885	(27 °C)	1.1723	(27 °C)	1.1762	(27 °C)
@	1.1778	(-180 °C)	1.1662	(-180 °C)	1.1625	(-180 °C)
Vcc=3.3 V	1.1629	(-230 °C)	1.1519	(-230 °C)	1.1408	(-230 °C)
Icc (μ A)	139	(27 °C)	126	(27 °C)	130	(27 °C)
TC (ppm/°C)	17.1	(-50:27) °C	10.6	(-50:27) °C	7.8	(-50:27) °C
@	49.8	(-180:27) °C	57.6	(-180:27) °C	28.1	(-180:27) °C
Vcc=3.3 V	89.1	(-230:27) °C	118.4	(-230:27) °C	69.9	(-230:27) °C

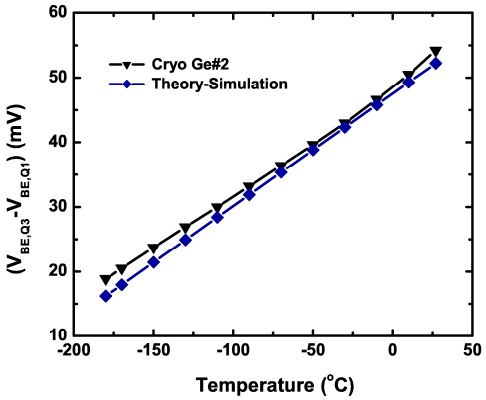

Fig. 6. Base-emitter voltage difference as a function of temperature.

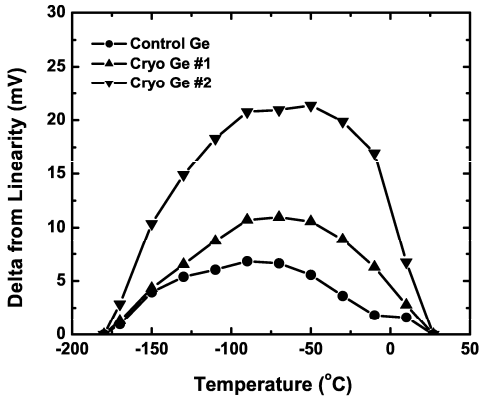

Fig. 7. Measured deviation from linearity for a SiGe HBT biased with a PTAT current for the three Ge profiles.

Measurements were performed using an Agilent 4155 Semiconductor Parameter Analyzer over a temperature range of 27 °C to –230 °C (the current limits of the cryostat system). The results are shown in Figs. 6-9.

The difference between the base-emitter voltages of transistors Q_2 and Q_1 was measured across temperature and is shown in Fig. 6. Ideally, this curve should follow equation (1) and should be linear over temperature. However, as reported in [3], the deviation from V_{BE} linearity for the two SiGe HBTs with different areas is different, resulting in a finite mismatch. As a result, the difference between the base-emitter voltages is not perfectly linear.

$$V_{BE,Q_2} - V_{BE,Q_1} = \frac{kT}{q}\ln(8). \qquad (1)$$

The deviation from V_{BE} linearity for transistor Q_3 as a function of temperature for the three Ge profiles is shown in Fig. 7. Note that the transistor is biased with a PTAT current. This deviation from linearity has usually been reported for the case when the transistor is biased at fixed collector current [3]. However, in many BGR topologies, the collector current for the transistors inside the circuit is instead the PTAT current. Calibrated 2-D simulations of the deviation from linearity for a single transistor with a size of Q_3, at fixed biased current and comparable collector-base voltage, are different from the measured results at the PTAT current for each of the three Ge profiles.

Measurement results show that the Cryo Ge #2 profile has the maximum deviation from linearity (at the PTAT current), while the Control Ge profile results in the minimum deviation from linearity over temperature, as expected.

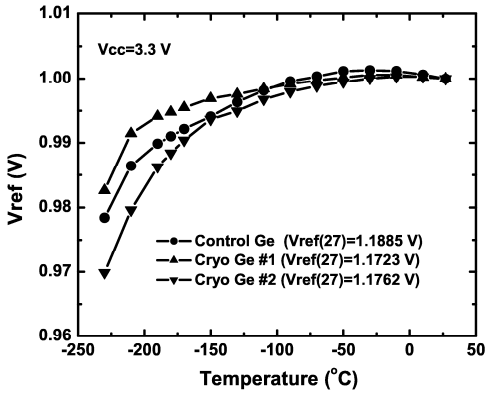

Fig. 8. Measured output voltage of the voltage reference as a function of temperature for three Ge profiles.

Fig. 8 shows the output voltage of the reference as a function of temperature for the three Ge profiles. The output voltage for each circuit was normalized by dividing it by its nominal voltage at 27 °C, for ease of comparison. It can be seen that circuits with Cryo Ge #2 and Cryo Ge #1 profiles have the best and the worst temperature stability among the three profiles, respectively, compared to the Control Ge profile. The temperature coefficients (TC in ppm/°C) for the 3 profiles are summarized in Table I. Our best case result of 28.1 ppm/°C for the cryo Ge profile #2 from

TABLE II
PERFORMANCE COMPARISON

	This Work	[7]	[8]	[2]	[9]	[10]
Technology	SiGe 5AM	SiGe 8HP	SiGe5HP	1.5 µm BiCMOS	6 µm CMOS	0.6 µm CMOS
Vcc (V)	3.3	2.5	2.5	5	-	2
Vref (V) @ 27 °C	1.172	1.026	1.328	1.264	1.192	1.142
TC (ppm/°C)	7.8 (-50:27) 28.1 (-180:27) 69.9 (-230:27)	8.4 (-50:27) 20.2(-180:27)	36.5(-50:150) 25.1 (0:75)	3.5 (0 :70) 8.9 (-55:125)	13.1 (0: 70) 25.6(-55:125)	5.3 (0: 100)

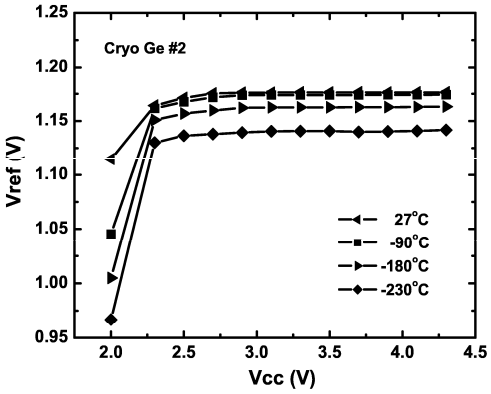

Fig. 9. Measured output voltage as function of power supply at 120 °C, 27 °C, -60 °C, -180 °C, and -230 °C for the Cryo Ge #2 profile.

27 °C to -180 °C, more than satisfies the required specifications for lunar systems.

The dependence of TC on Ge profile shape can be explained by reviewing the technique used here for curvature compensation. Referring to Fig. 4, the output voltage of the BGR is approximately by [2]

$$V_{ref}(T) \approx V_{BE,Q_3}(T) + K_1 R_2 T + K_1 R_2 T / \beta(T) \quad (2)$$

where T is the absolute temperature, R_2 is the resistor in the last circuit branch, and K_1 and K_2 are coefficients corresponding to the PTAT currents. Note that both $V_{BE,Q3}$ and the current gain (β) depend on the shape of the Ge profile in the base, thus affecting the overall output temperature dependence of the reference output [3]-[6]. The temperature dependence of the current gain, in particular, is used to minimize the temperature drift of the output voltage. Detailed expressions for $V_{BE,Q3}$(T) and β (T) for SiGe HBTs as a function of Ge profile shape can be found in [4], and when combined with (2) are generally consistent with our measurements.

Fig. 9 shows the change in the output voltage as the power supply changes, at five different temperatures, for the Cryo Ge #2 version of the reference circuit. As can be seen, the line regulation remains well-behaved across the extreme temperature range.

A comparison of the BGRs presented in this work with the existing state-of-the-art ([2],[7]-[10]) across a more standard operating temperature range is given in Table II. It is expected that the circuits in [2],[9] and [10] will not function down to -180 °C.

V. Summary

We have presented results on SiGe BiCMOS precision voltage references designed for operation across extreme temperature ranges (+120 °C to -180 °C). Our best case voltage reference achieves a 28.1 ppm/°C temperature coefficient over +27 °C to -180 °C, more than adequate for the intended lunar electronics applications, suggesting that SiGe technology is an ideal candidate for such space exploration applications.

VI. Acknowledgement

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