

A Monolithic, Wide-Temperature, Charge Amplification Channel for Extreme Environments

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Abstract—This paper describes the design, implementation, and characterization of a monolithic charge amplification channel for use as a piezoelectric sensor front-end in extreme environment applications.¹² The design leverages a 50 GHz peak- f_T SiGe BiCMOS technology platform to achieve functionality across a wide-temperature range from -180°C to 120°C . As part of a much larger remote electronics unit, the channel is specified to amplify piezoelectric transducer signals with frequencies up to 5 kHz and amplitudes as low as 200 pC. Intended for use in lunar surface systems, the application requires the capability to absorb up to 100 krad(SiO_2) of total ionizing dose (consistent with a typical lunar mission cycle) and be hardened against latch-up effects that cause system failure in a heavy ion radiation environment. Preliminary characterization of the channel shows the desired integration of an AC current input, programmable gain, and effective filtering at three distinct cutoff frequencies.

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1. INTRODUCTION

“Extreme environment” electronics has emerged as an important field of research in the space community and is focused on eliminating the high costs associated with protecting electronic systems from harsh environmental conditions. Wide temperature swings (e.g., -180°C (night) to $+120^\circ\text{C}$ (day) on the surface of the Moon) and constant exposure to ionizing radiation currently necessitate the use of shielded “warm boxes” to maintain functional systems in

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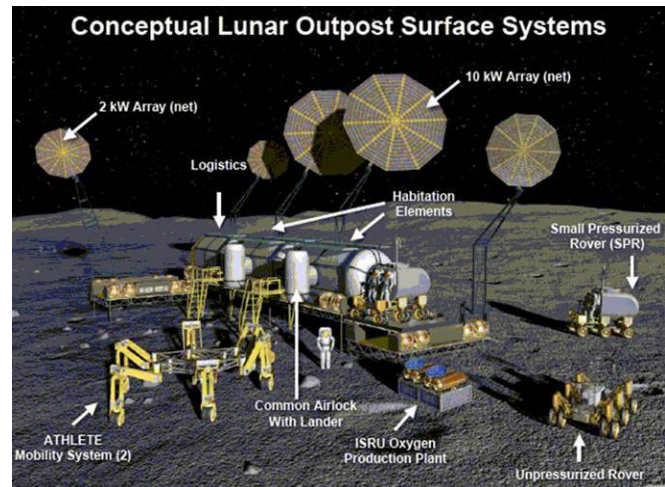


Figure 1 – Conceptual depiction of surface systems likely to be developed for the operation of a lunar outpost.

these environments and limit the ability to create truly distributed, modular solutions. Figure 1 depicts an artist’s concept of surface systems likely to be utilized in an operational lunar outpost. The intrinsic properties of commercially-available silicon-germanium (SiGe) BiCMOS platforms make them uniquely suited for designing monolithic systems capable of operating in extreme environments [1].

The SiGe Integrated Electronics for Extreme Environments research group (SiGe EEE) was established under the NASA Exploration Technology Development Program (ETDP) to develop electronic systems in state-of-the-art SiGe platforms to meet the challenges posed by complex initiatives such as lunar colonization. The Remote Health Node (RHN), originally designed at BAE Systems for the X-33 spacecraft, was chosen as a starting point in order to demonstrate the numerous advantages that can be leveraged in an integrated BiCMOS process. The original design, shown in Figure 2, sought modularity by combining multiple types of sensor interfaces into a single hardware implementation usable throughout a spacecraft or exploration vehicle to provide mission critical data to engineers in an efficient, reliable manner [2]. Advancing this concept one step further, the SiGe EEE team has developed an integrated version of the RHN, not only reducing form-factor and power by substantial margins, but also completely eliminating the need for isolation from the environment [3]. The entire SiGe Remote Electronics Unit

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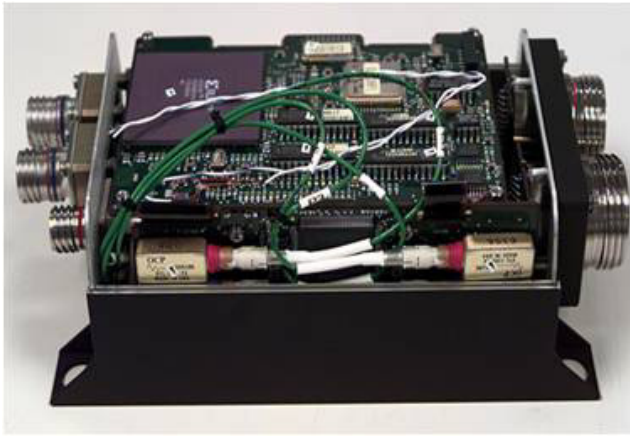


Figure 2 – Original implementation of the Remote Health Node developed by BAE Systems.

(REU) is designed to be housed within a single connector (Figure 3) or multi-chip package, and utilized throughout the spacecraft or surface vehicle as required by a mission's sensor payload.

Piezoelectric sensing represents one of many common applications that stand to benefit from such a modular system design approach. This paper describes the design and measurement of a SiGe charge amplification channel developed as a part of the much larger Remote Electronics Unit (REU) for space system avionics platforms. The channel was designed in a 1st generation SiGe technology platform as a fully monolithic solution, with the exception of the passive network required for charge amplification. The signal path consists of a low-offset, high-input impedance op-amp, a variable gain control, calibration, and offset compensation through an 8-bit voltage DAC. Special consideration was given to wide-temperature biasing, which is provided in part by an exponential curvature-compensated bandgap reference. The layout occupies a total area of 2.61 x 0.84 mm² and consumes only 13.2 mW of power. This represents a significant improvement over the original RHN design.

2. TECHNOLOGY PLATFORM

The BiCMOS technology chosen for the development of the Remote Electronics Unit was the IBM SiGe 5AM platform, which integrates a 50 GHz, self-aligned *npn* HBT into a 0.5 μm CMOS process. An SEM cross-section of the SiGe HBT is shown in Figure 4. The platform includes 1.35 fF/ μm^2 metal-insulator-metal (MIM) capacitors, low temperature-coefficient polysilicon resistors, and four layers of metallization for routing, including a thick, analog copper top metal. While the SiGe HBT used in the process has been shown to possess favorable performance metrics at low temperatures due to the beneficial effects of the Ge-grading-induced drift field [1], it was still necessary in initial phases

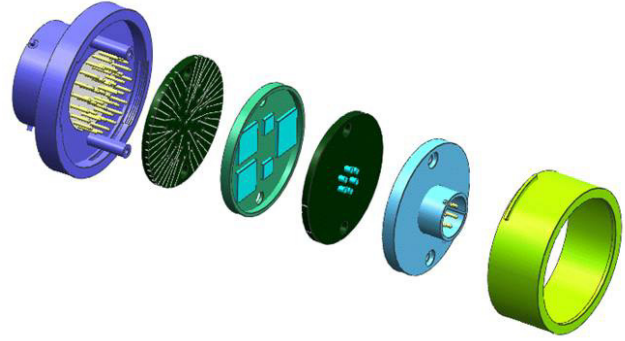


Figure 3 – Rendering of the new Remote Electronics Unit connector housing.

of the project to produce accurate, reliable models for both the SiGe HBT and CMOS devices used in the design for temperature ranges well beyond those available in the basic IBM process (-55°C to 120°C).

In addition to wide-temperature performance, reliability of active devices at cryogenic temperatures was carefully examined in early phases of the project. It has been shown that SiGe HBTs exhibit robust operation under stress at both cryogenic and high temperatures with no indication of reliability degradation [4]. It is well documented, however, that the performance of nFET devices can be compromised by hot carrier effects (HCE), and that these effects are exacerbated at cryogenic temperatures [5]. To mitigate this potential reliability issue and to simultaneously reduce leakage effects from radiation-induced shallow-trench oxide interface traps, a minimum nFET gate length of 1 μm was enforced for all designs. No such requirement was enforced for the gate lengths of the pFETs, as they are inherently less susceptible to both HCE and leakage effects caused by ionizing radiation exposure. SiGe HBTs have also been

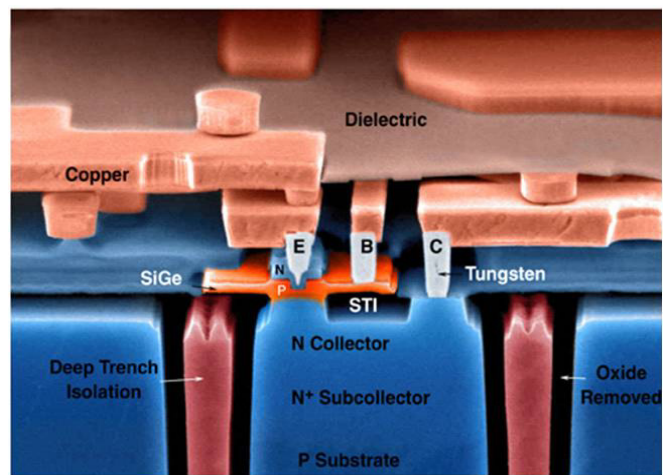


Figure 4 – SEM cross-section of a SiGe HBT [1].

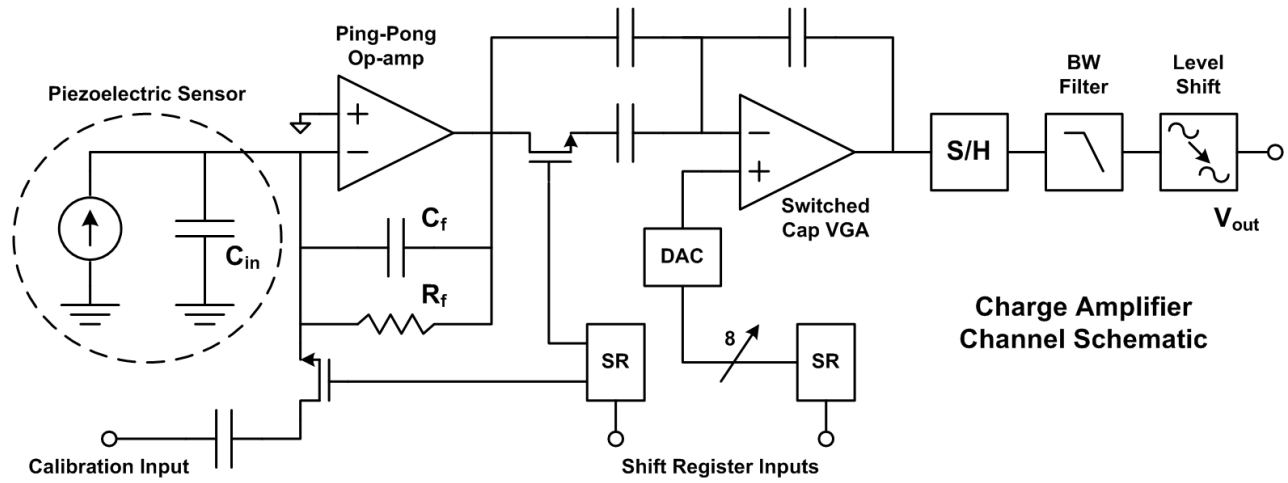


Figure 5 – Schematic design of the full charge amplifier channel, including a basic lumped element model for the piezoelectric sensor input.

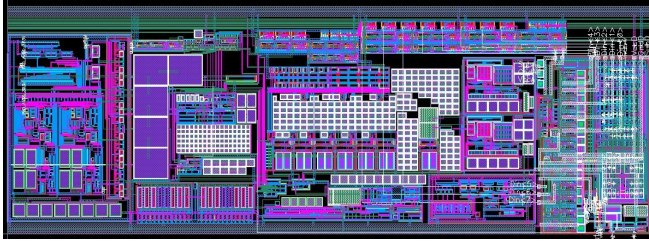


Figure 6 – Complete charge amplifier layout.

shown to possess resilience to total ionizing dose effects, due primarily to the vertical structure of the device, where dose levels exceeding 1 Mrad(SiO₂) have produced little observable effect in device performance (both DC and AC) at bias levels of interest [6], [7]. nFETs do not share this tolerance, however, and some consideration for bias levels with respect to expected radiation dose is required in order to ensure that the drain-source leakages at the edges of the shallow trench isolation (STI) do not adversely affect circuit performance. In general the nFETs in this technology do not exhibit enough performance degradation up to the specified 100 krad(SiO₂) to pose a major challenge for circuit design, and the previously mentioned 1 μm minimum gate length imposed for the project serves to mitigate the issue even further.

Consideration also had to be given to the susceptibility of BiCMOS circuits to potential latch-up events caused by heavy ion irradiation. When p-type and n-type (nFET or HBT) devices are placed in close proximity, latch-up can occur when the parasitic transistor formed between the pFET n-well and the n-type devices enters a high-current, positive feedback state [8]. Particularly in a radiation environment, an ion strike to the vicinity of this parasitic transistor can cause a latch-up state to occur where it may not have in a terrestrial setting. Careful layout techniques, including liberal use of n-well contacts, substrate contacts, and guard bands, were used throughout the circuit designs to harden against this phenomenon.

3. CHANNEL ARCHITECTURE

A charge amplifier functions by converting charge stored on a capacitor to voltage at its output node. The nature of this process allows a charge amplifier to maintain signal integrity in highly capacitive environments that would normally prohibit a voltage amplifier from properly functioning due to strong attenuation of the AC data presented by the sensor. The range of applications for such amplifiers is broad. The advantages are illustrated simply by considering a system in which the sensor and amplifier cannot be placed in close proximity. A charge amplifier's inherent insensitivity to input load capacitance, C_{in} , allows it to process signals across long lengths of capacitive cabling and provide flexibility and modularity to an otherwise limited system. These advantages are leveraged to good effect in extreme environments, where distributed signal processing may not always be practical [9].

The complete charge amplifier channel architecture is shown schematically in Figure 5 with the finalized 2.62 x 0.86 mm² layout shown in Figure 6. The design is based loosely on the original BAE implementation consisting entirely of off-the-shelf components. The new charge amplifier is fully monolithic, with the exception of the feedback resistor and capacitor (R_f and C_f) on the channel front-end. For charge amplification, the output voltage is determined to first order solely by the amount of charge provided by the sensor and the size of the amplifier's feedback capacitance, as:

$$V = Q_{in} / C_f \quad (1)$$

Constrained by the need to amplify relatively large charge amplitudes at low frequencies with a maximum rail voltage of 3.3 V, a 33 nF capacitor and a 10 MΩ resistor were chosen for the feedback network, neither of which could be fabricated on-chip within a reasonable die area. Details of the individual integrated circuit blocks are found in the sections that follow.

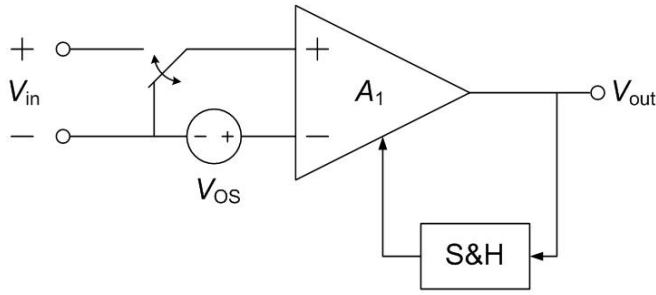


Figure 7 – Block diagram representation of the autozeroing technique [10].

Ping-Pong Amplifier Input Stage

A fundamental requirement for precision charge amplification is to present a high input impedance to the output of the piezoelectric sensor such that charge loss to the input of the initial gain stage is minimized. The finite current gain of bipolar devices (available in a BiCMOS process) make them less effective in this respect, so an amplifier design with a common-source, nFET input stage was chosen to act as the channel's front-end. In previous design iterations, it was also determined that offset would represent one of the biggest challenges in the channel architecture. Within BAE's off-the-shelf solution, offset was easily negated with coupling capacitors between each gain stage. Unfortunately, monolithic designs are not capable of integrating the large capacitors required for low frequency AC coupling due to the large silicon die areas they require. Application of a technique known as auto-zeroing (AZ) was used to mitigate this issue.

Figure 7 depicts a block level diagram of the AZ technique as described by Enz and Temes in [10]. Cancellation of offset is accomplished by sampling the shorted inputs of the operational amplifier (switch closed) to determine the input referred V_{os} . This value is stored on a capacitor in the sample-and-hold block such that when V_{in} is sampled, the stored voltage is subtracted from the amplified output. The end effect is cancellation of the internal offset of the amplifier and a substantial reduction in $1/f$ noise. Despite these advantages, some increase in the noise floor will be introduced due to aliasing of the transients generated by the switching process [10].

Because the amplifier operates in two distinct phases, sampling and amplifying, it is not inherently capable of utilization in a continuous-time application. Conversion of the AZ architecture to a continuous time solution was accomplished by implementing the ping-pong configuration depicted in Figure 8. The topology consists of two identical AZ amplifiers, switch networks, sample-and-hold filters, and switch drivers. When switched out of phase, at any given time one of the amplifiers is sampling its offset while the other is amplifying its autozeroed input. As a whole, the amplifier acts in a continuous fashion [11], [12]. Measured results across temperature are shown in Figure 9, with the

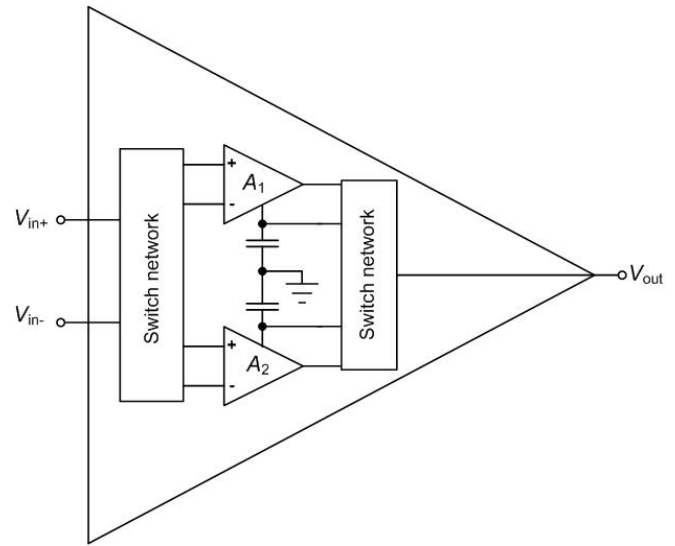


Figure 8 – Block diagram of the ping-pong auto-zero operational amplifier [12].

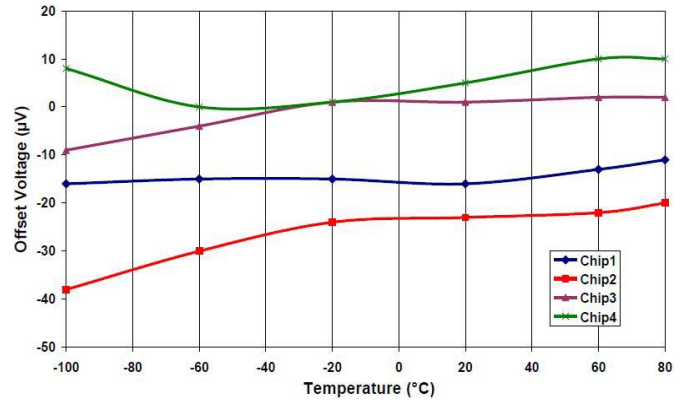


Figure 9 – Offset vs. temperature measured for four ping-pong op-amps [9].

complete frontend exhibiting no more than 40 μV of offset across a 180°C temperature range. Details of the individual circuit blocks are fully described in [13].

Switched Capacitor Variable Gain Amplifier

Applying the same auto-zeroing principles utilized in the ping-pong front end, the second stage of the charge amplifier channel minimizes voltage offset using a feedback path to a nulling input. The schematic design is shown in Figure 10. Two gain states ($A_V = 10$ and $A_V = 50$) are realized in the capacitive feedback network, with the high gain feedback path being programmable through an nFET gate controlled by one of the two shift registers used in the channel. The other MOS gates are clocked continuously by signals from a clock generator that takes a single-ended 83.125 kHz signal and produces the various phases necessary to alternate the amplifier between its zeroing and amplification states. In the sampling state, the output of the main amplifier is fed back through a secondary opamp where the offset voltage is stored on C_{null} . This voltage is

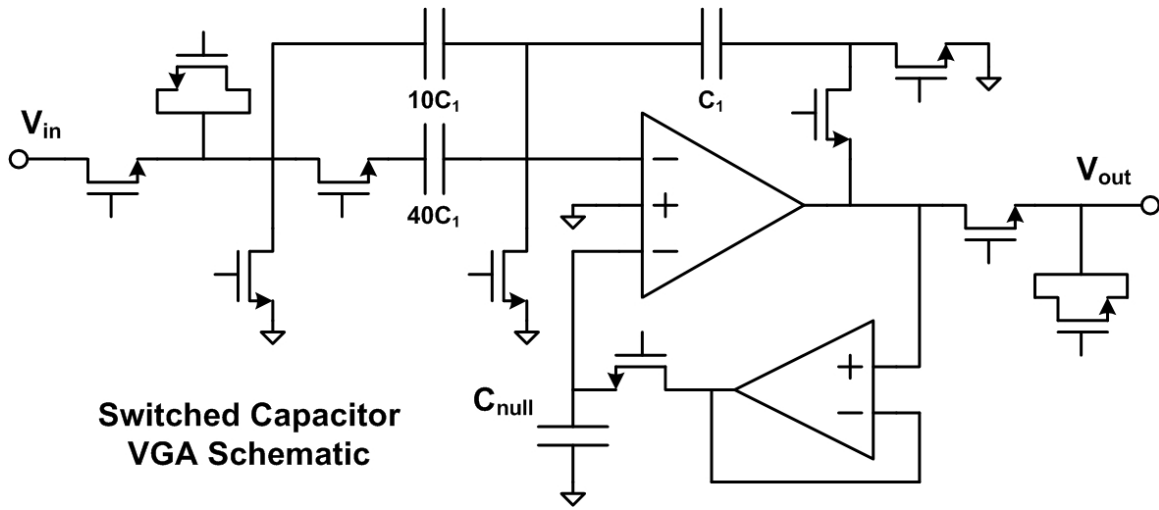


Figure 10 – Schematic design of the switched capacitor variable gain amplifier.

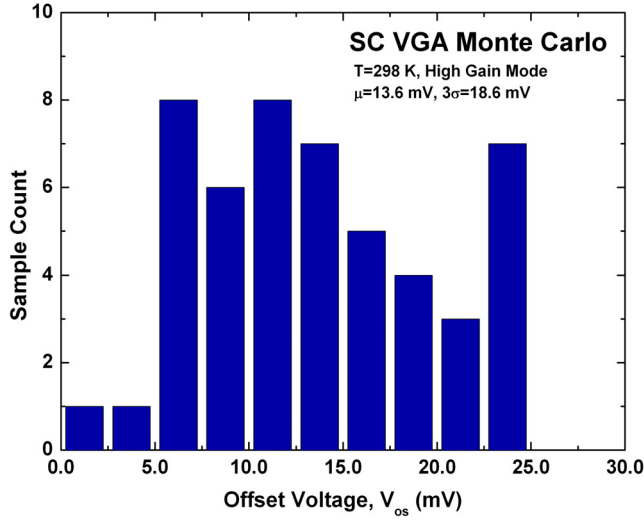


Figure 11 – Monte Carlo (25 samples) offset voltage simulation results for the SC VGA in high gain mode.

then cancelled during the amplification phase by a nulling differential pair in the main amplifier [10]. Figure 11 shows Monte Carlo offset results for 25 samples, taking into account normal process variation. The simulations show an average offset of 13.6 mV.

In a final effort to guarantee that the charge channel signal following amplification would not “rail” in any gain configuration, the reference voltage provided for the entire switched capacitor VGA was produced from an 8-bit calibration DAC controlled by the second programmable shift register (shown in Figure 5). The voltage DAC was designed for stability across the full temperature specification and produces a stable, adjustable reference that calibrates out offset drift in the channel caused by variation. Unlike the input stage, the VGA does not employ a ping-pong architecture, in order to allow continuous temperature swings, ionizing radiation damage, and process amplification. Instead, the output is filtered by a sample-

hold amplifier switched out of phase with the VGA before it is sent to the Butterworth filter.

Sixth Order Switched Capacitor Butterworth Filter

The original specification for the charge amplifier channel called for programmable filtering at three distinct cutoff frequencies up to 5 kHz. To this effect, a 6th order low-pass switched capacitor Butterworth filter was designed, and serves to filter high-frequency signals such as the switching noise introduced by the previous channel stages and to prevent aliasing of the ADC that processes the channel output. The Butterworth architecture is a popular method for designing high-order and high-selectivity (high-Q) filters and operates by transforming the desired transfer function into cascaded first- and second-order stages. It has the advantage of reduced sensitivity to quantization of its coefficients and provides good phase response [14].

The Butterworth filter schematic is shown in Figure 12. Its three bi-quad stages utilize custom op-amps with MIM capacitor feedback networks. The MOS switches are controlled by a clock divider circuit that produces the clock phases necessary for its operation. The final implementation of the channel utilizes three clock frequencies for the Butterworth filter (665 kHz, 332.5 kHz, and 83.125 kHz) which are divided by a clock-to-cutoff frequency ratio of 100:1. A standalone version of the filter was extensively tested across the full specified temperature range (-180°C to 125°C) with consistent results attributable to the use of temperature stable biasing techniques, as described in the next section. The output of the Butterworth feeds a post-filter composed of a single op-amp and feedback network. The post-filter places two poles above the corner frequency to assist in the reduction of clock feed through [14].

Wide-Temperature Bandgap Reference

The development of stable biasing techniques represents one of the most important challenges in the design of reliable integrated circuits for extreme environments. These

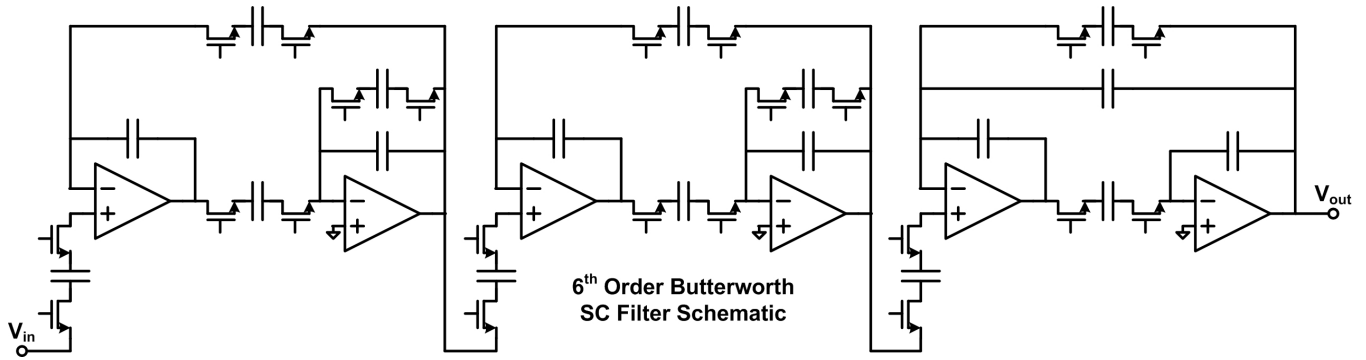


Figure 12 – Schematic design of the sixth order Butterworth switched capacitor filter [14].

references serve as the foundation upon which the rest of the system relies, and it is of the utmost importance to ensure that they are designed with the specific needs of each analog circuit block in mind. A designer's success in this area is heavily dependent on the quality of the available device models, and most often these models do not remain accurate below the lowest military temperature specification of -55°C . For the scope of this project, the development of models preceded any subsequent work on analog circuits.

The BiCMOS voltage reference most heavily utilized in the charge channel was first conceived by Lee [15] and consists of an exponentially curvature-compensated design which uses the inverse relationship of an HBT's base-emitter voltage (V_{be}) to temperature to compensate the typical behavior of a proportional to absolute temperature (PTAT) current source. This design was refined and tested in the current technology platform in [16], and is shown schematically in Figure 13. The output voltage, taken from the positive side of R_2 , can simply be defined as:

$$V_{out} = I_{PTAT}R_2 + V_{be,Q1} \quad (2)$$

As ambient temperature rises, the current provided by the PTAT current source and mirrored through R_2 rises proportionately. The placement of Q_1 , however, allows the exponential decrease in V_{be} with temperature to compensate. In this way, the design is able to maintain a stable output voltage across extremely wide temperature ranges. The BGR fabricated for this project was tested from -180°C to 27°C , achieving an impressive best case temperature coefficient of $28.1 \text{ ppm}/^{\circ}\text{C}$ [16].

4. CHANNEL CHARACTERIZATION

Preliminary verification of channel functionality was performed with the full analog remote sensor interface, including all sixteen channels and the analog-to-digital converter, wirebonded into a 121-pin grid array package (PGA). The package was mounted onto a custom designed printed circuit board and stimulated using a Keithley 6221 AC Current Source. The chip was designed to receive all of its clocking and control signals from the remote digital control interface, but it was necessary to provide those signals externally prior to proving functionality of the full REU. National Instrument's *SignalExpress* software package was used to provide synchronized clocks and data strings to the various components, while the SC VGA and Butterworth clocks were supplied by a Tektronix AFG3252 Arbitrary Function Generator.

Figure 14 shows functionality of the programmable offset correction built into the switched capacitor VGA. Each consecutive waveform represents an increment of four in the calibration shift register. For the purpose of the measurement, the channel was operating in low gain mode with an input square wave frequency of 1 kHz and amplitude of $2.5 \mu\text{A}$. Integration of this square wave by the charge amplifier front end produces the familiar triangle wave output seen in the plot. The full scale voltage range following the level shifter at the end of the channel is 0 to 1.2 V , which is required by the design of the ADC. This data, and all subsequent data presented in this paper, were taken at room temperature.

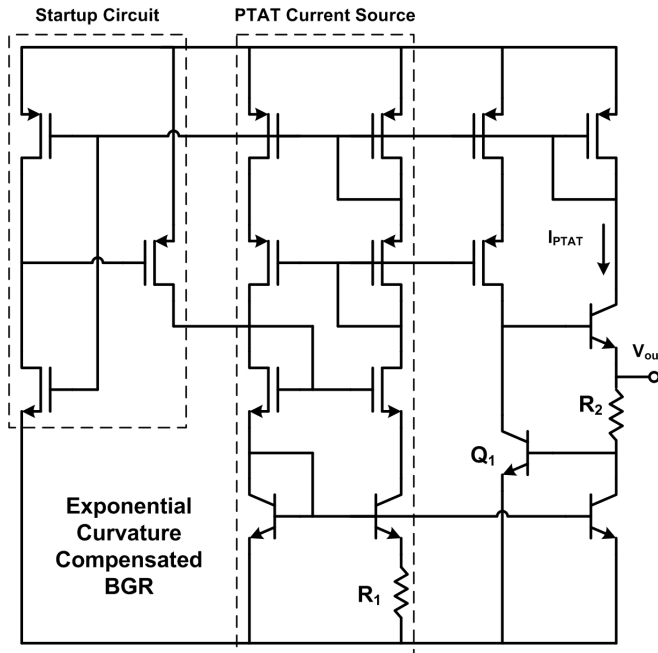


Figure 13 – Schematic design of the exponential curvature-compensated bandgap reference.

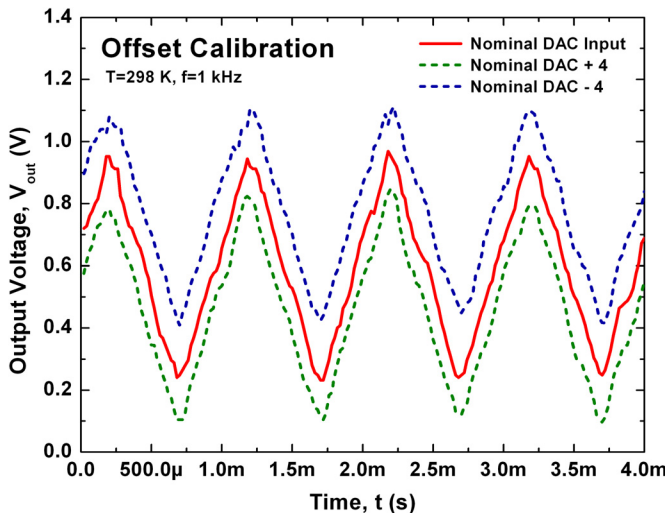


Figure 14 – Output voltage vs. time showing the offset calibration capability of the SC VGA.

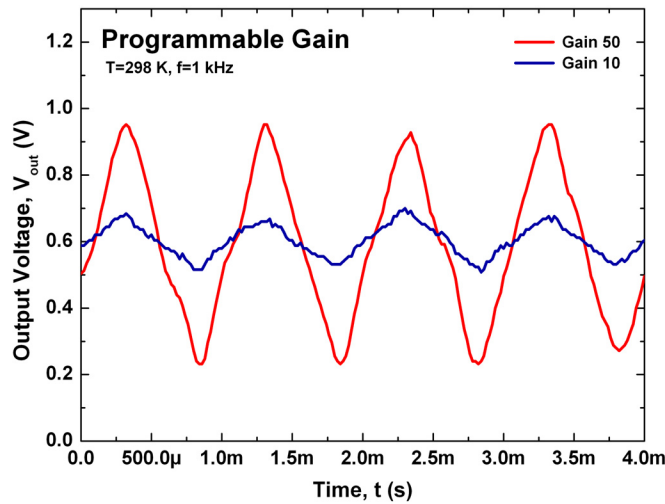


Figure 15 – Output voltage vs. time showing the channel's programmable gain functionality.

In Figure 15, waveforms are shown for each of the gain states of the charge channel. Both originated from a 1 kHz, 500 nA square wave input. The noise that is apparent in the low-gain waveform is caused, at least partially, by the long signal lines required to measure the charge channel stand-alone. In the completed multi-chip module (presently in fabrication), it is expected that noise levels will decrease substantially. Figure 16 depicts all three filtering frequencies of the Butterworth filter in operation. The 1 kHz input signal is not attenuated for the two higher corner frequency cases. As the corner frequency dips below 1 kHz, however, the higher frequency harmonics are removed and the output is converted to a sine wave.

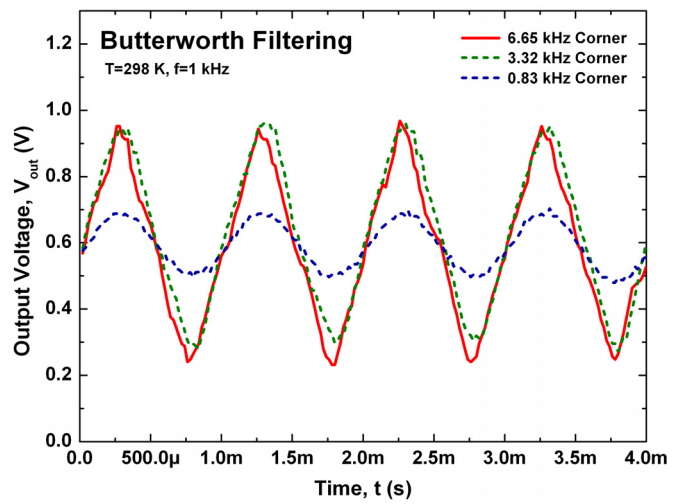


Figure 16 – Output voltage vs. time showing three Butterworth corner frequency settings.

5. SUMMARY

This paper has described the design and measurement of a programmable, charge amplification channel for use as a piezoelectric sensor front-end in extreme environments. As a part of the 16-channel remote analog sensor interface shown in Figure 17, the channel was designed to be fully monolithic (with the exception of the front-end feedback) and to operate reliably in the environmental conditions present on the lunar surface. These conditions include temperatures ranging from -180°C to 120°C and ionizing radiation exposure not to exceed 100 krad(SiO₂) over a complete mission cycle. The channel was designed to amplify charge signals as small as 200 pC up to frequencies of 5 kHz using two programmable gain states, offset calibration, and programmable filtering. Preliminary characterization of the circuit has proven its basic functionality in all respects.

The channel, and the entire remote electronics unit described, stands to offer significant advantages to mission engineers seeking to reduce payload, power consumption, and ultimately cost, while enjoying the benefits of a temperature and radiation hardened BiCMOS technology. The unprecedented modularity of the solution will ultimately provide valuable flexibility in the placement of sensors and sensor interfaces to monitor all manner of systems critical to the health of a mission. Future measurement tasks specific to the charge channel will include characterization across the full temperature spectrum, determination of figures-of-merit such as noise floor and input charge signal range, and radiation tolerance (both total dose and single event).

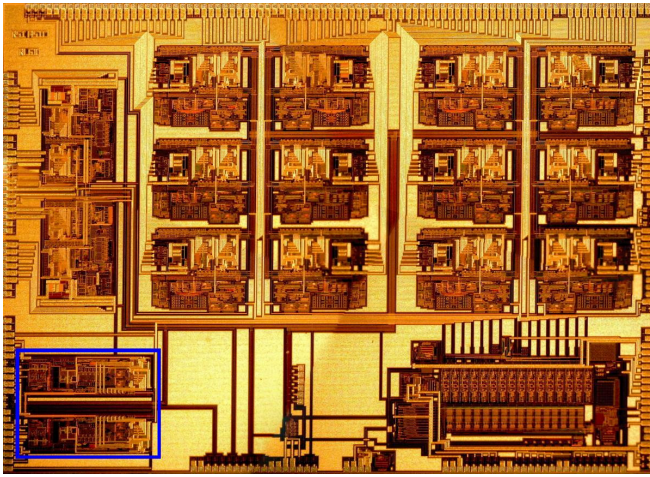


Figure 17 – Fully integrated, 16-channel analog remote sensor interface with two charge channels highlighted (bottom left).

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BIOGRAPHY



Ryan Diestelhorst is a Ph.D. student in Electrical Engineering at the Georgia Institute of Technology, Atlanta, GA. He received his B.Sc. and M.Sc. degrees from Georgia Tech in Electrical and Computer Engineering in 2006 and 2008, respectively. His research is focused on analog and mixed-signal integrated circuit design for extreme environment applications, in which he has developed successful techniques in SiGe BiCMOS technology platforms for both device-level radiation hardening and wide-temperature circuit operation. He has worked with the SiGe EEE Team under the NASA ETDp project for three years, leading Georgia Tech's contribution to the project in areas from circuit level design and layout to wide-temperature characterization and radiation testing of complete system architectures. He has 15 publications in the field, and has presented novel device and circuit hardening techniques twice at the IEEE Nuclear and Space Radiation Effects Conference.



Steven Finn is an Analog Circuit Design Engineer with National Semiconductor. His recent works have focused on high-speed data path circuit design including CDR and SERDES development. He previously completed a Master of Science in Electrical Engineering from Georgia Tech in 2008

where he performed circuit design research under Dr. John Cressler relating to extreme-environment applications.



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